

# Electrical Properties of Amorphous-Indium-Gallium-Zinc-Oxide Based Thin-Film Transistors with Four Terminal Configuration

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## ABSTRACT

This study extracted the intrinsic device properties of indium-gallium-zinc-oxide (IGZO) thin-film transistors (TFTs) from four terminal (4T) measurements and compared them with the extrinsic properties which were deduced from conventional two terminal (2T) measurements to explore the effects of any resistances, including the source/drain metal contacts and the channel, on the IGZO TFT properties. For operation in the linear region at low  $V_{DS}$ , the intrinsic channel ( $R_{Ch-intrinsic}$ ) and contact resistances ( $R_{C-intrinsic}$ ), which were higher than the extrinsic channel ( $R_{Ch-extrinsic}$ ) and contact ones, respectively, were of the same order of magnitude (183 k $\Omega$  at  $V_{GS} = 10$  V), indicating that the operation of the TFTs is governed by both the intrinsic channel and intrinsic contact resistances. The developed TFTs also exhibited an intrinsic 4T linear mobility of 4.4 cm<sup>2</sup>/Vs, which is about 61% lower than the extrinsic 2T one. This was attributed to the higher value of  $R_{Ch-intrinsic}$  compared to  $R_{Ch-extrinsic}$ .

**KEYWORDS:** Indium-Gallium-Zinc-Oxide Thin-Film Transistors, Four Terminal (4T) Configuration, Two Terminal (2T) Measurements, Intrinsic Device Properties, Extrinsic Properties.

## 1. INTRODUCTION

Recently, amorphous indium gallium zinc oxide (a-IGZO) thin-films have been widely used as a channel layer in the fabrication of flexible low-cost thin film transistors (TFTs), because of their high field-effect mobility, as well as their simplicity, low-cost, and high throughput.<sup>1–9</sup> In order to explore the actual potential distribution in the channel region, the scanning Kelvin probe microscopy (SKPM)<sup>7,10</sup> and four terminal configuration (FTC)<sup>6–9,11</sup> methods have been used for organic TFTs and a-Si:H TFTs and the transmission line (TL)<sup>12</sup> method has been employed for amorphous oxide semiconductor (AOS) TFTs. In the SKPM method, however, the minimum voltage resolution is worse than that of a conventional semiconductor analyzer and the voltage signal is distorted by topography signals.<sup>7</sup> Furthermore, the TL method cannot provide accurate electrical properties for AOS-TFTs operated at low  $V_{DS}$  values, owing to the large channel parameter dispersion.<sup>7,12</sup> On the other hand, the FTC method is the best technique for the accurate measurement of the electrical properties of AOS-TFTs. Prior reports for a-IGZO TFTs with a four

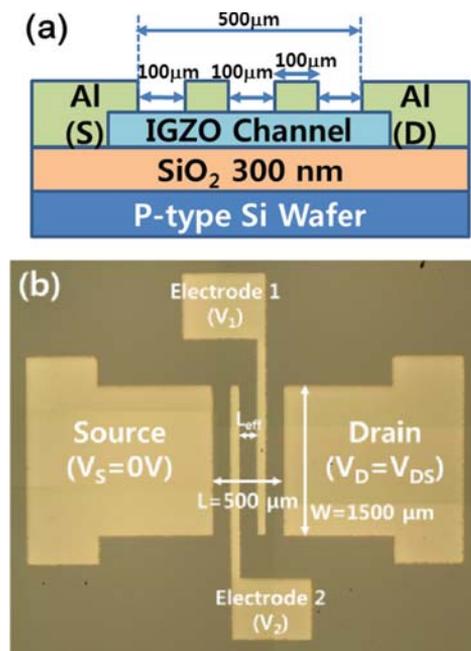
terminal configuration employed a simple analytical model based on the gate bias-dependent mobility,<sup>6</sup> extracted the intrinsic parameters of the TFTs for a fixed  $L$  at room temperature,<sup>7</sup> and then later on as functions of  $L^9$  and temperature.<sup>8</sup> Contrary to these prior works, we used a simple aluminum source and drain metal electrodes and utilized a short channel length, only five times larger than the width of the probe electrode, to explore its effect on the results of the four terminal (4T) measurement for a-IGZO TFTs with FTC. In this study we made a comparison between conventional two terminal (2T) TFT measurements and those which involve two additional electrodes in the channel region (4T) for a-IGZO TFTs with FTC to investigate the effects of the contact resistance between the source/drain and the channel.

## 2. EXPERIMENTAL DETAILS

IGZO channel layers were deposited at 250 °C for 1 hour on 300-nm-thick SiO<sub>2</sub> films grown on (100) Si substrates from an IGZO target with an atomic ratio of In:Ga:Zn = 1:1:1 by RF magnetron sputtering. A mixture of Ar and oxygen (O<sub>2</sub>) gases with flow rates of 22.5 and 7.5 sccm, respectively, was used as the reaction gas. The working pressure was fixed at 5 mTorr during deposition and the SnO target power was fixed at 50 W. The typical thickness

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Received: 23 November 2015  
Accepted: 25 August 2016

of the IGZO channel layers was approximately 50 nm. SiO<sub>2</sub> and the a-IGZO layers were post-annealed at 150 °C for 1 hour in O<sub>2</sub> ambient after deposition. To prepare the patterned source and drain electrodes, aluminum (Al) films were deposited on top of the IGZO channel layers by DC magnetron sputtering and patterned by wet etching. The Ar flow rate was 20 sccm, the working pressure was fixed at 0.5 mTorr during deposition and the input voltage was fixed at DC 100 V. The thickness of the Al electrodes was 150 nm and the width (*W*) and length (*L*) of the fabricated samples were 1500 μm and 500 μm, respectively. Figures 1(a and b) show the schematic cross-sectional and photographic top views, respectively, of the typical samples prepared in this study. As shown in Figure 1, the TFTs have a bottom gate and a top contact structure. For the a-IGZO TFTs with FTC, there are two additional electrodes in the channel region. All of the distances from the source to electrode 2, between the two electrodes, and from electrode 1 to the drain are the same, with a value of 100 μm. The effective distance and voltage drop between electrodes 1 and 2 are denoted as *L*<sub>eff</sub> and *V*<sub>1</sub>–*V*<sub>2</sub>, respectively. The device characteristics of the IGZO-based TFTs with FTC were measured at RT in a darkened probe box in air using two Keithley 2400 source meters at the DC voltage source and a Keithley 6485 picoammeter for the current measurements along with the corresponding software (Microsoft visual basic). The capacitances of the



**Fig. 1.** (a) Schematic cross-sectional view and (b) photographic top view of sputter-deposited IGZO-TFTs with four terminal configuration (FTC) developed in this study: *W* = 1500 μm and *L* = 500 μm. The effective distance and the voltage drop between electrodes 1 and 2 are denoted as *L*<sub>eff</sub> and *V*<sub>1</sub>–*V*<sub>2</sub>, respectively.

SiO<sub>2</sub> gate dielectric films were measured at RT using an Agilent 42854A precision LCR meter after forming Ohmic contacts with a 150-nm-thick Al layer by DC sputtering.

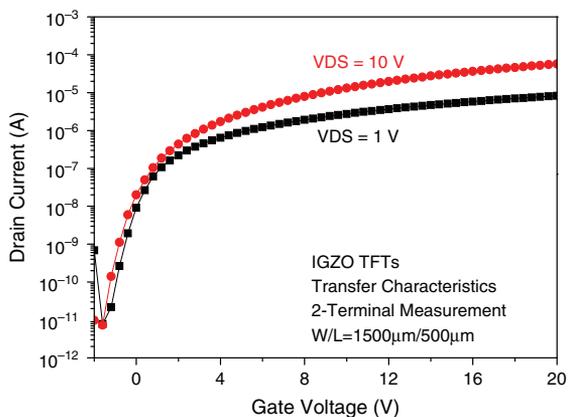
### 3. RESULTS AND DISCUSSION

Figure 2 shows the typical drain-to-source current versus the gate-to-source voltage (*I*<sub>DS</sub>–*V*<sub>GS</sub>) transfer curves of the sputter-deposited IGZO-based TFTs obtained from the 2T measurements. A series of measurements were performed with the drain-to-source voltage (*V*<sub>DS</sub>) varied from 1 to 10 V, which are values well within the linear and saturation regions, respectively. As shown in Figure 2, the onset voltage (*V*<sub>ON</sub>) (*V*<sub>ON</sub>, defined as *V*<sub>GS</sub> at which the mobile hole carriers begin to accumulate in the channel and the *I*<sub>DS</sub> begins to increase in a transfer curve) shifted slightly to the left for the two *V*<sub>DS</sub> values of 1 and 10 V.

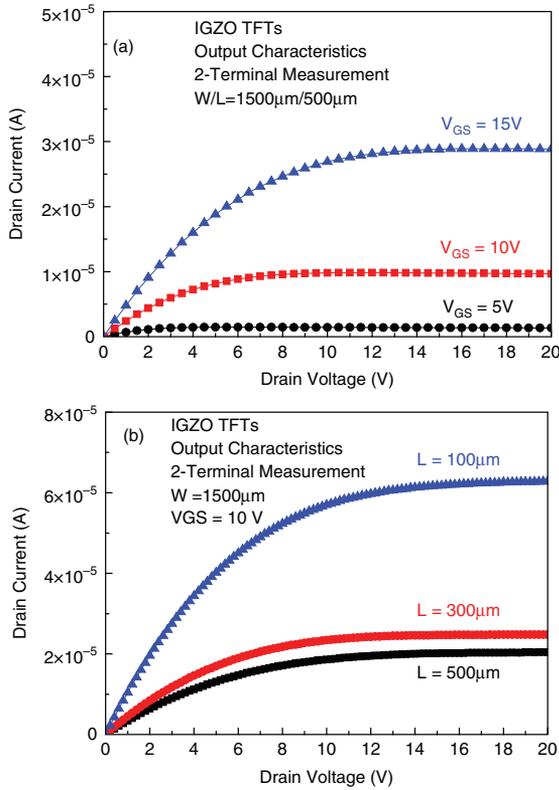
The typical *I*<sub>DS</sub>–*V*<sub>DS</sub> output curves of the sputter-deposited IGZO-based TFTs as a function of *V*<sub>GS</sub> and *L* obtained from the 2T measurements are shown in Figure 3. As can be seen in Figure 3, the output characteristics revealed that there is no current crowding effect, which indicates the existence of close to ohmic contacts between the IGZO channel and Al source/drain electrode. Therefore, it was observed from Figures 2 and 3 that the developed TFTs showed well-behaved TFT characteristics. The data in Figure 3 was also employed to extract the extrinsic TFT parameters of the IGZO TFTs by the linear fitting of the plot of the total TFT resistance (*R*<sub>Tot</sub>) as a function of *L*.

We used the channel resistance method to deduce the extrinsic devices parameters of the IGZO TFTs and assumed that *R*<sub>Tot</sub> can be estimated using Eq. (1)

$$R_{\text{Tot}}(V_{\text{GS}} - V_{\text{ON}}) = \frac{V_{\text{DS}}}{I_{\text{DS}}(V_{\text{GS}} - V_{\text{ON}})}$$



**Fig. 2.** Typical *I*<sub>DS</sub>–*V*<sub>GS</sub> transfer curves of sputter-deposited IGZO-based TFTs obtained from 2T measurements. *V*<sub>DS</sub> was varied from 1 V to 10 V, which are values well within the linear and saturation regions, respectively.



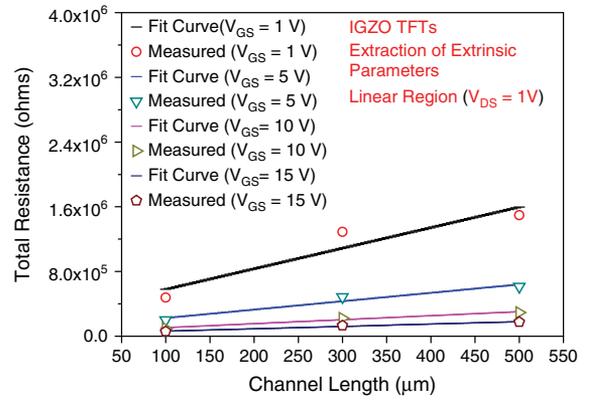
**Fig. 3.** Typical  $I_{DS}-V_{DS}$  output curves of sputter-deposited IGZO-based TFTs as a function of (a)  $V_{GS}$  and (b) channel length,  $L$ , obtained from 2T measurements. The data in this figure was employed to extract the extrinsic TFT parameters of the IGZO TFTs by linear fitting of the plot of the total resistance as a function of  $L$ .

$$= R_{Ch-extrinsic}(V_{GS} - V_{ON}) + R_{C-extrinsic}(V_{GS} - V_{ON})$$

$$= R'_{Ch-extrinsic}(V_{GS} - V_{ON}) \times L + R_{C-extrinsic}(V_{GS} - V_{ON}) \quad (1)$$

where  $R_{Ch-extrinsic}$  and  $R_{C-extrinsic}$  are, respectively, the extrinsic channel resistance and the contact resistance of the source/drain electrode contacts, including any other parasitic resistances at the source/drain ends, and are supposed to be a function of  $V_{GS}-V_{ON}$ .  $R'_{Ch-extrinsic}$ , which is independent of the channel length, was also separated from  $R_{Ch-extrinsic}$ . Here,  $V_{ON}$  rather than the threshold voltage was used, because it is determined mainly by the trapped charges, whereas shifts in the threshold voltage in TFTs can be related to changes in many more physical parameters, such as the sub-threshold swing (SS) and mobility.<sup>13,14</sup> In order to determine the extrinsic parameters,  $R'_{Ch-extrinsic}$  and  $R_{C-extrinsic}$ , the  $R_{Tot}$  characteristics of the IGZO TFTs operating in the linear region at  $V_{DS} = 1$  V as functions of  $L$  at various  $V_{GS}$  values were plotted using the results in Figure 3 and are shown in Figure 4. Here,  $R'_{Ch-extrinsic}$  and  $R_{C-extrinsic}$  are extracted from the slope and intercept of the linear fitting, as shown in Figure 4.

Figures 5(a and b) show the plots of the inner-electrode voltages,  $V_1$  and  $V_2$ , as a function of  $V_{GS}$  measured at



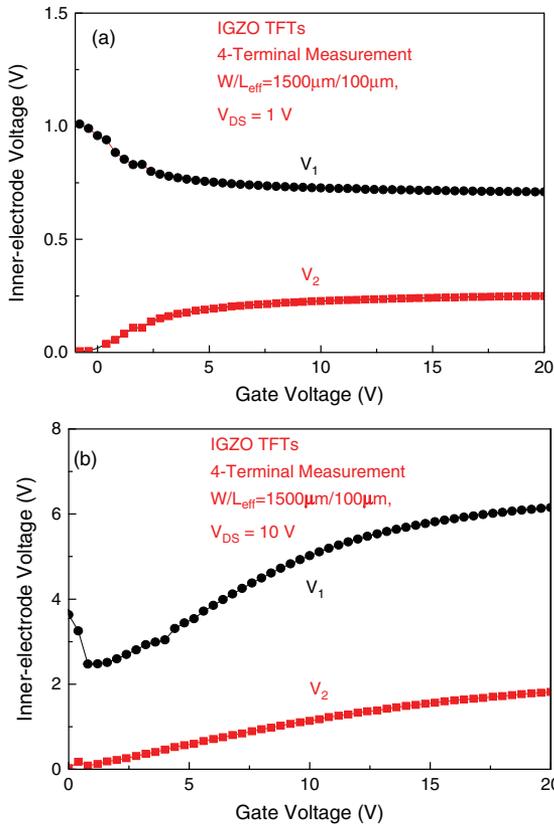
**Fig. 4.**  $R_{Tot}$  characteristics of IGZO TFTs as functions of  $L$  at various  $V_{GS}$  values for a given  $V_{DS}$  of 1 V to determine the extrinsic parameters of  $R'_{Ch-extrinsic}$  and  $R_{C-extrinsic}$  as given in Eq. (1). Here,  $R'_{Ch-extrinsic}$  and  $R_{C-extrinsic}$  are extracted from the slope and intercept of the linear fittings.

$V_{DS} = 1$  (linear region) and 10 V (saturation region), respectively.  $V_1$  and  $V_2$  are the voltages at electrodes 1 and 2, respectively, as shown in Figure 1. The voltage drop between these two electrodes represents the true intrinsic channel voltage unaffected by the source/drain contact resistances, due to the fact that electrodes 1 and 2 sense only the voltage, but not the current, and there is no current flow through these two electrodes. At  $V_{DS} = 1$  V, as is seen in Figure 5(a), the inner-electrode voltages in the on-region at  $V_{GS} > 5$  V are constant at  $V_1 = 0.73$  V and  $V_2 = 0.23$  V, which are about three fourths and one fourth of  $V_{DS}$ , respectively. In this case, the channel is in a strong accumulation state with a small Debye length, which leads to an electrical disconnection between the back channel region and the gate electrode.<sup>3</sup> Thus, the inner-electrode voltages are related to the potential distribution, which depends mainly on  $V_{DS}$ . This suggests that the intrinsic channel resistance ( $R_{Ch-intrinsic}$ ) is almost uniform throughout  $L$  in the linear operation region for low  $V_{DS}$  values ( $\ll V_{GS}-V_{ON}$ ) and indicates that the intrinsic contact resistances ( $R_{C-intrinsic}$ ) at the source/drain metal contacts are low compared with  $R_{Ch-intrinsic}$ . At  $V_{DS} = 10$  V, as is seen in Figure 5(b), the inner-electrode voltages increase linearly with  $V_{GS}$  from 1 to 10 V, and become saturated at  $V_{GS} > 10$  V, suggesting that the channel region is affected not only by  $V_{DS}$ , but also by  $V_{GS}$ , in saturation mode. Based on the result in Figure 5, we can determine that the best  $V_{GS}$  (or  $V_{GS}-V_{ON}$ ) values for an FTC analysis, in order to deduce the intrinsic device parameters accurately, are in the range from 5 to 10 V.

We also used the channel resistance method to extract the intrinsic devices parameters of the IGZO TFTs and modified  $R_{Tot}$  in Eq. (1) as follows:

$$R_{Tot}(V_{GS} - V_{ON})$$

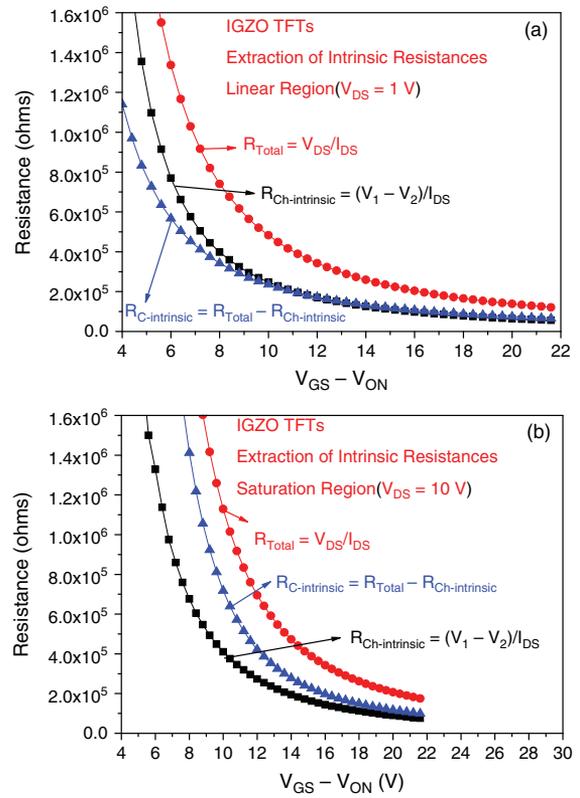
$$= \frac{V_{DS}}{I_{DS}(V_{GS} - V_{ON})}$$



**Fig. 5.** Characteristics of the inner-electrode voltages,  $V_1$  and  $V_2$ , as a function of  $V_{GS}$  measured at (a)  $V_{DS} = 1$  V (linear region) and (b)  $V_{DS} = 10$  V (saturation region).  $V_1$  and  $V_2$  are the voltages at electrodes 1 and 2, respectively (see Fig. 1).

$$\begin{aligned}
 &= R_{Ch-intrinsic}(V_{GS} - V_{ON}) + R_{C-intrinsic}(V_{GS} - V_{ON}) \\
 &= \frac{V_1 - V_2}{I_{DS}(V_{GS} - V_{ON})} + R_{C-intrinsic}(V_{GS} - V_{ON}) \quad (2)
 \end{aligned}$$

where  $R_{Ch-intrinsic}$ , which is given by  $(V_1 - V_2)/I_{DS}$ , is the intrinsic channel resistance,  $V_1 - V_2$  is the measured voltage difference between electrodes 1 and 2, and  $R_{C-intrinsic}$  is the intrinsic contact resistance, which is related to the source/drain electrode contacts. Figures 6(a) and (b) show the intrinsic parameters of  $R_{Ch-intrinsic}$  and  $R_{C-intrinsic}$  as a function of  $V_{GS} - V_{ON}$  for  $V_{DS} = 1$  V (linear region) and  $V_{DS} = 10$  V (saturation region), respectively. The intrinsic parameters are extracted from the results in Figure 5 using Eq. (2). As shown in Figure 6, at low  $V_{GS} - V_{ON}$  values in the range from 5 to 10 V,  $R_{Ch-intrinsic}$  is larger than  $R_{C-intrinsic}$  (575 k $\Omega$  compared with 453 k $\Omega$  at  $V_{GS} - V_{ON} = 6.8$  V) and this small difference vanishes quickly as the  $V_{GS} - V_{ON}$  value increases in linear operation mode, while  $R_{C-intrinsic}$  is much larger than  $R_{Ch-intrinsic}$  (2.34 M $\Omega$  compared with 0.97 M $\Omega$  at  $V_{GS} - V_{ON} = 6.8$  V) and this larger difference disappears slowly with increasing  $V_{GS} - V_{ON}$  value in saturated operation mode. This suggests that the linear mode

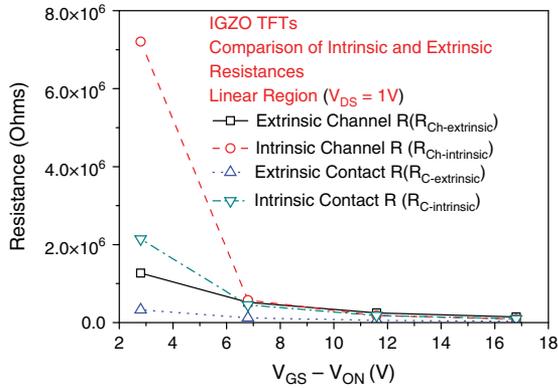


**Fig. 6.** Characteristics of intrinsic channel resistance,  $R_{Ch-intrinsic}$ , and intrinsic contact resistance,  $R_{C-intrinsic}$ , as a function of  $V_{GS} - V_{ON}$  for (a)  $V_{DS} = 1$  V (linear region) and (b)  $V_{DS} = 10$  V (saturation region). The intrinsic parameters are extracted from the results in Figure 5 using Eq. (2).

operation is governed more effectively by the intrinsic channel resistance, although the effect of the intrinsic contact resistance is not negligible, whereas the saturation region operation is influenced mainly by the intrinsic contact resistance, which is closely related to the voltage distribution between the two inner-electrodes, as shown in Figure 5.

We also compared the extrinsic resistances of the IGZO TFTs, which were extracted from the 2T measured results in Figure 4 using Eq. (1), with the intrinsic ones which were deduced from the 4T measured results in Figures 5 and 6 using Eq. (2). This comparison is provided in Figure 7. As shown in this figure, for operation in the linear region at low  $V_{DS} = 1$  V,  $R_{Ch-intrinsic}$  and  $R_{C-intrinsic}$  are higher than  $R_{Ch-extrinsic}$  and  $R_{C-extrinsic}$ , respectively, and are about the same order of magnitude (183 k $\Omega$  at  $V_{GS} - V_{ON} = 11.6$  V). This indicates that the operation of the TFT in linear mode is governed by the intrinsic channel and intrinsic contact resistances.

In the case of the 2T measurements, the extrinsic (2T) linear mobility,  $\mu_{lin-extrinsic}$ , where the difference between



**Fig. 7.** Comparison of characteristics between extrinsic channel/contact resistances ( $R_{Ch-extrinsic}/R_{C-extrinsic}$ ) and intrinsic channel/contact resistances ( $R_{Ch-intrinsic}/R_{C-intrinsic}$ ) of IGZO TFTs as a function of  $V_{GS}-V_{ON}$  for  $V_{DS} = 1$  V (linear region). The extrinsic resistances were extracted from the 2T measured results in Figures 3 and 4 by using Eq. (1), while the intrinsic ones were deduced from the 4T measured results in Figures 5 and 6 by using Eq. (2).

the gate and threshold voltages,  $V_{GS}-V_{TH}$ , is greater than  $V_{DS}$ , is given by

$$\mu_{lin-extrinsic} = \frac{\partial I_{DS}}{\partial V_{GS}} \frac{L}{W} \frac{1}{C_{SiO_2}} \frac{1}{V_{DS}} \quad (3)$$

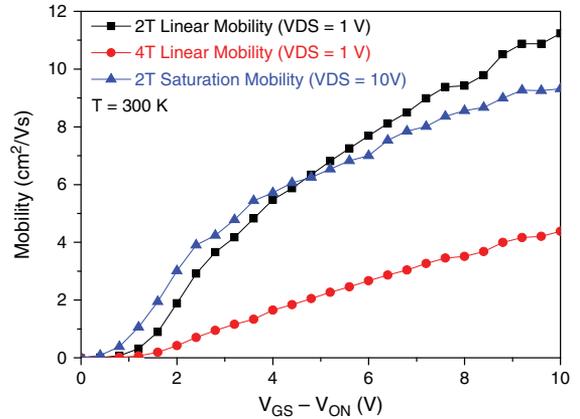
where  $C_{SiO_2} = 11.5$  nF/cm<sup>2</sup> is the capacitance per unit area of the SiO<sub>2</sub> dielectric measured using a metal-insulator-metal structure. If  $V_{GS}-V_{TH} < V_{DS}$ , then the device operates in saturation mode and the extrinsic saturation mobility,  $\mu_{sat-extrinsic}$ , is calculated from

$$\mu_{sat-extrinsic} = \left( \frac{\partial \sqrt{I_{DS}}}{\partial V_{GS}} \right)^2 \frac{2L}{W} \frac{1}{C_{SiO_2}} \quad (4)$$

With the 4T measurements, only the voltage difference,  $V_1-V_2$ , within the effective channel length,  $L_{eff}$ , is considered, thereby excluding the intrinsic (4T) contact resistance at the S/D electrode-IGZO interface. Thus, with a slight modification of Eq. (3), the intrinsic linear mobility,  $\mu_{lin-intrinsic}$ , can be estimated from<sup>6,7,9,15</sup>

$$\mu_{lin-intrinsic} = \frac{\partial I_{DS}}{\partial V_{GS}} \frac{L_{eff}}{W} \frac{1}{C_{SiO_2}} \frac{1}{(V_1 - V_2)} \quad (5)$$

The different device mobilities at room temperature derived using the above Eqs. (3)–(5) from the results shown in Figures 2 and 5 are provided in Figure 8 as a function of  $V_{GS}-V_{ON}$ . The applied  $V_{GS}$  was corrected by  $V_{ON}$  to ensure that the mobilities at various gate voltages are accurately determined.<sup>16</sup> As shown in Figure 8, the extracted mobility values increased with increasing  $V_{GS}-V_{ON}$  and the developed TFTs exhibited a  $\mu_{lin-intrinsic}$  value of 4.4 cm<sup>2</sup>/Vs at  $V_{GS}-V_{ON} = 10$  V, which is about 61% lower than the  $\mu_{lin-extrinsic}$  value (11.2 cm<sup>2</sup>/Vs) extracted from the 2T measurements. This disparity between the intrinsic 4T



**Fig. 8.** The extrinsic 2T saturation ( $\mu_{sat-extrinsic}$ ), the extrinsic 2T linear ( $\mu_{lin-extrinsic}$ ), and the intrinsic 4T linear mobilities ( $\mu_{lin-intrinsic}$ ) at room temperature as a function of  $V_{GS}-V_{ON}$  estimated with Eqs. (3)–(5) from the results shown in Figures 2 and 5. It is shown that the magnitude of the mobility decreases in the order  $\mu_{lin-extrinsic} > \mu_{sat-extrinsic} > \mu_{lin-intrinsic}$  for  $V_{GS}-V_{ON}$  values ranging from 5 to 10 V.

linear and extrinsic 2T linear mobilities can be explained by the higher values of  $R_{Ch-intrinsic}$  and  $R_{C-intrinsic}$  compared to  $R_{Ch-extrinsic}$  and  $R_{C-extrinsic}$ , respectively, as is evident in Figure 7. In the linear regime, the high intrinsic channel and contact resistances reduce the measured intrinsic 4T linear mobility considerably, while under 2T measurements, the much lower  $R_{C-extrinsic}$  than  $R_{C-intrinsic}$  results in improved charge carrier injection from the S/D electrodes and a larger measured extrinsic 2T mobility value. In contrast to our present results, a recent study<sup>9</sup> reported that the intrinsic linear mobility was about 20% higher than that derived from 2T measurements for a-IGZO TFTs, resulting from the lower value of  $R_{Ch-intrinsic}$  compared to  $R_{Ch-extrinsic}$ . In our sample, the width of the two additional electrodes is large ( $\sim 100$   $\mu$ m) enough compared with the channel length (500  $\mu$ m) and the channel potential is affected by the probe electrode, resulting in the higher value of  $R_{Ch-intrinsic}$  compared to  $R_{Ch-extrinsic}$ , which indeed leads to a lower  $\mu_{lin-intrinsic}$  than  $\mu_{lin-extrinsic}$ .

#### 4. CONCLUSION

We extracted the intrinsic parameters, such as the resistances and mobility, of IGZO-TFTs from 4T measurements and compared them with the extrinsic ones which were deduced from 2T measurements, in order to explore the effects of any resistances, including the source/drain metal contacts and the channel, on the TFT properties. We used the channel resistance method to deduce these intrinsic and extrinsic parameters. We concluded that the linear mode operation is governed more effectively by the intrinsic channel resistance, although the effect of the intrinsic contact resistance is not negligible, whereas the saturation operation is influenced

mainly by the intrinsic contact resistance. The developed TFTs exhibited a  $\mu_{\text{lin-intrinsic}}$  value of 4.4 cm<sup>2</sup>/Vs at  $V_{\text{GS}} - V_{\text{ON}} = 10$  V, which is about 61% lower than the  $\mu_{\text{lin-extrinsic}}$  value (11.2 cm<sup>2</sup>/Vs) extracted from the 2T measurements. This disparity between the intrinsic 4T linear and extrinsic 2T linear mobilities can be explained by the higher values of  $R_{\text{Ch-intrinsic}}$  and  $R_{\text{C-intrinsic}}$  compared to  $R_{\text{Ch-extrinsic}}$  and  $R_{\text{C-extrinsic}}$ , respectively.

**Acknowledgment:** This work was supported by the Industrial Strategic Technology Development Program (10041596, Development of core technology for TFT free active matrix addressing color electronic paper with day and night usage), funded by the Ministry of Trade, Industry and Energy (MI, Korea).

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