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LTPO TFT Technology for Level Shifter Integrated Gate Driver in UHD 4K Displays

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Abstract

We demonstrate the level shifter integrated gate drive circuits using Low-Temperature Poly-Si (LTPO) TFT technology. Three level shifters are integrated with a 16-stage 2-clock CMOS shift register. A low 5 V start pulse is level up to a high 20 V for gate driving operation. The 4 μs pulse width ensures its speed compatibility to drive an Ultra-High Definition (UHD) 4K displays (3840 X 2160 @ 60 Hz).

Author Keywords

LTPO TFT; Level Shifter; Shift Register; Gate Driver.

1. Introduction

Low-Temperature Poly-Si (LTPO) thin-film transistor (TFT) technology is becoming a new sensation for the Active Matrix Organic Light-Emitting Diodes (AMOLED) and Ultra-High-Definition (UHD) displays [1]. Usually the oxide TFT exhibits ultra-low off-state leakage current < 10^{-14} A, decent high mobility over 10 cm^2/V.s, and can be manufactured at low temperature with low manufacturing cost [2]. LTPS TFT is proud of high mobility and excellent stability [3] although high off-state current (~ 10^{-12} A) still reckons a weak point. By integrating these two TFT technologies it is possible to crisscross the disadvantages and take the advantages from both sides.

The performance enhancement with the LTPO TFT technology has been reported with various circuits like pixel circuits [1], level shifter [2], inverter [4]-[5], operational amplifier [6], and TFTs array [7]. However, gate drive circuits with this technology not yet realized to the best of our knowledge. In very recent, we report a high-speed and wider swing level shifter (LS) through this technology [2]. In this work, we fabricate a 16-stage 2-clock conventional CMOS shift register (SR). The LS is integrated with the SR to realize a low voltage driven integrated CMOS gate drive circuits. The circuit is compatible to drive 4K displays.

2. Experimental detail

The LTPO TFTs were fabricated on the glass substrate (Fig. 2(a)). P-type LTPS TFT with coplanar structure and n-type dual-gate a-IGZO TFTs with back-channel etch (BCE) structure were fabricated. For the p/n active 100 nm poly-Si and 40 nm, a-IGZO was utilized. Mo layer is used for the gate and source/drain electrodes. For the passivation layer, 250 nm SiO_2 layer is deposited through plasma-enhanced chemical vapor deposition (PECVD). Finally, the devices are annealed at 250 ºC for 4h in a vacuum. Details of the coplanar single gate and dual gate TFT process are studied in our previous reports [8]-[9]. More details of the 6-mask LTPO fabrication process described in [2], [4]-[5]. The electrical properties of the TFTs were measured at room temperature using the Agilent 4156C semiconductor analyzer. Input pulses to the level shifter, shift register, and integrated gate driver circuits were provided by the function generator and the output is obtained through the oscilloscope measured data.

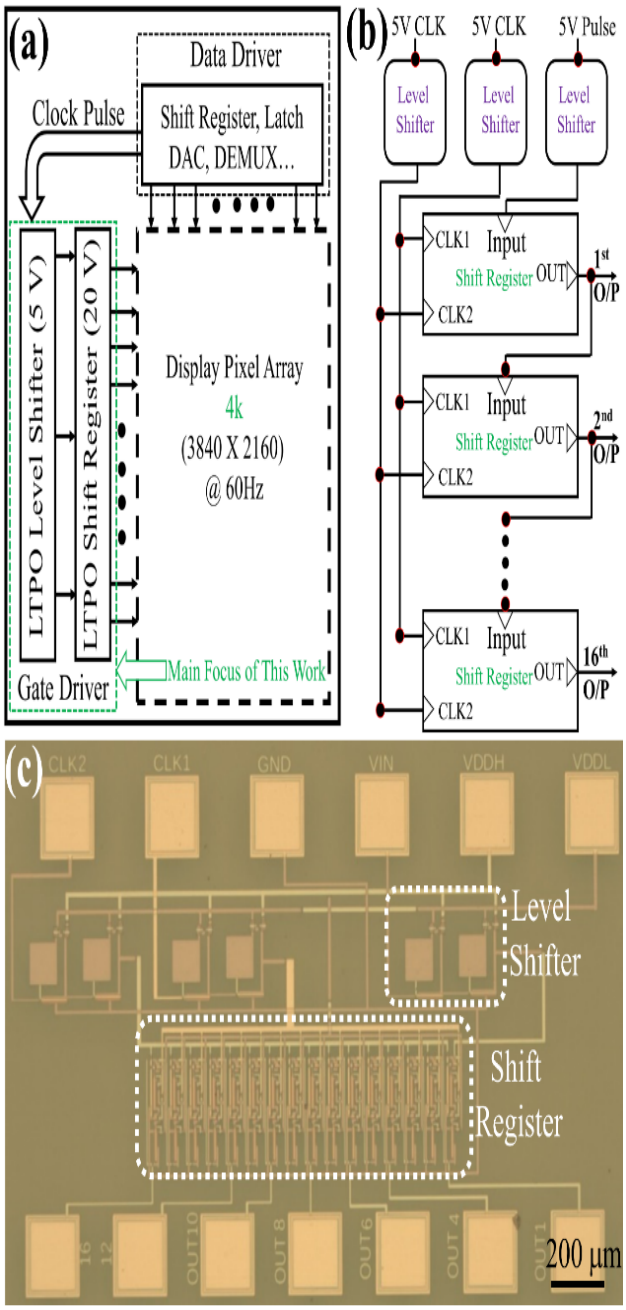

Figure 1. (a) Simplified representation of a display panel where the 'main focus of this work' is marked on. Schematic diagram of the level shifter integrated gate drive circuit (b), and the optical image of the whole circuit (c).

3. Results and discussion

Fig. 1 (a) shows the simplified representation of a display panel where the 'main focus of this work' is marked on. Schematic diagram of the level shifter integrated gate drive circuit 1 (b), and optical image of the whole circuit 1 (c).

In Fig. 2. the schematic for LTPO TFTs (a). Measured transfer characteristics of 2 (b) p-type LTPS TFT with W/L of 20/6 µm, and 2 (d) n-type dual-gate a-IGZO TFT with W/L 100/6 µm. The inset shows the optical image of the fabricated TFTs accordingly. The output characteristics of the respected TFTs are shown in 2 (c) and 2 (e). The p-type TFT exhibits V_{th} of -1.2 V, $\mu_{fe\text{-}max}$ of 80 cm^2/V.s, and SS of 0.7 V/dec. The n-type DG a-IGZO TFT exhibits the V_{th} of 0.9 V, SS of 0.28 V/dec., and $\mu_{fe\text{-}max}$ of 14 cm^2/V.s.

Fig. 3. The circuit schematic for LTPO level shifter (a), and optical image of the fabricated device 3 (b). SPICE simulated signals at different nodes of the LS are shown in 3 (c). The oscilloscope measured data for level conversion of (10V- 30V) at 25 kHz is shown in 3 (d). The LS exhibits a fast rise time of 740 ns (Fig. 3(d)) and operational in the broad clock frequency range of (1- 500) kHz. For an input swing of (2-10) V, the LTPO LS shows a shifted output swing of (10-30) V with the full 'rail-to-rail' character [2].

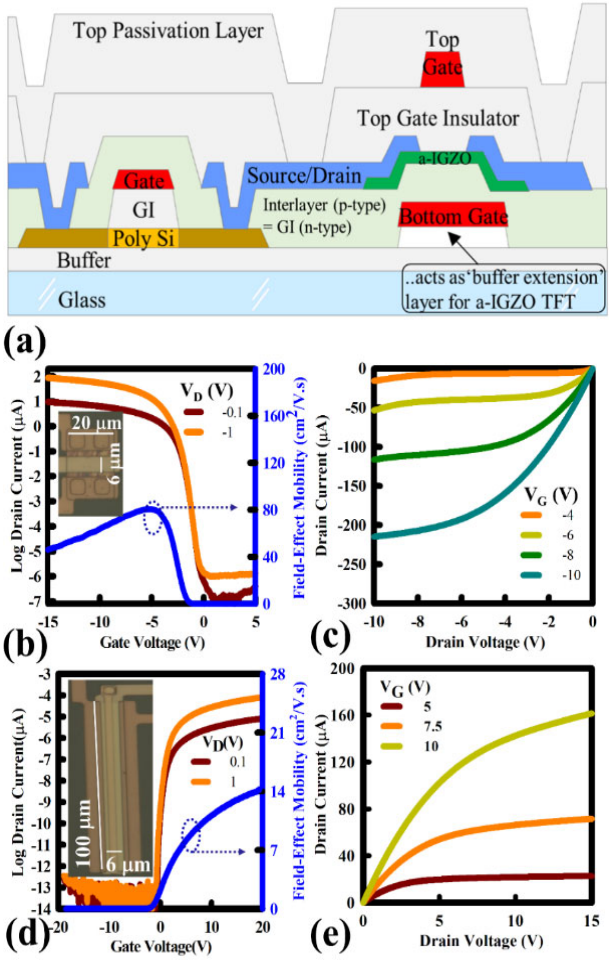

Figure 2. The schematic for LTPO TFTs (a). Measured transfer characteristics of (b) p-type LTPS TFT with W/L of 20/6 µm, and (d) n-type dual-gate a-IGZO TFT with W/L 100/6 µm. The inset shows the optical image of the fabricated TFTs accordingly. The output characteristics of the respected TFTs are shown in (c) and (e).

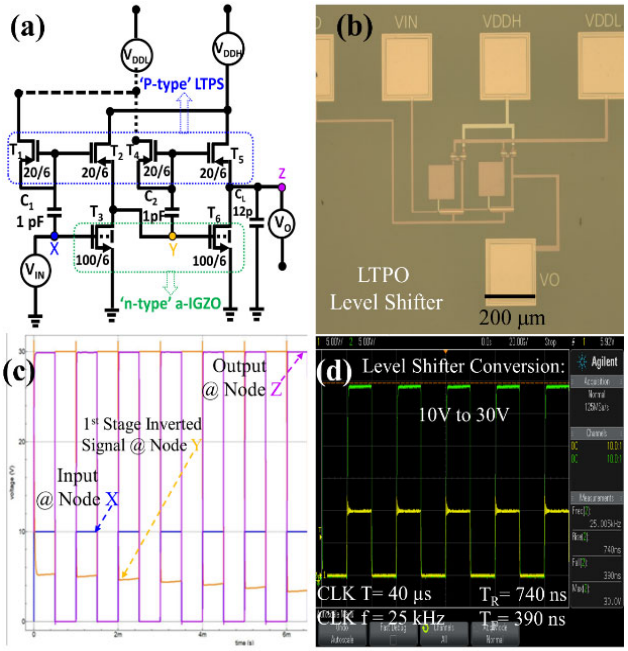

Figure 3. The circuit schematic for LTPO level shifter (a), and the optical image of the fabricated device (b). SPICE simulated signals at different nodes of the LS are shown in (c). The oscilloscope measured data for level conversion of (10V- 30V) at 25 kHz is shown in (d).

Fig. 4. Conventional CMOS 2-clock shift register's single-stage TFT structured diagram 4 (a), and the optical image 4 (b). The measured output response of the shift register (SR) at the different stages are plotted in 4 (c) for a 4 µs, 15 V input pulse. The pitch and width of the SR for a single-stage are 78 µm and 285 µm respectively. The rise and fall time for the SR is < 1 µs which is fast enough.

Fig. 5. LTPO CMOS level shifter integrated gate driver measured performance for the operation frequency of 250 kHz. For a low 5V start pulse to the high 20V output, driving is shown for the 1st stage 5 (a), 4th stage 5 (b), 8th stage 5 (c), and 16th stage 5 (d). All output stages are functional. A 4K display contains about 4000 horizontal scan lines. Start pulse with a width of 4 µs is compatible with this speed.

Previously, level shifter integrated gate driver is realized with a-Si TFTs [10], a-IGZO depletion-mode TFTs [11]-[12] or with LTPS TFTs [13]. Mono TFT technologies [10]–[13], show poor operation frequency performance. For example with a-Si TFT gate drive circuits works in 5 kHz [10] and using a-IGZO TFTs it only increases to 12.5 kHz [11]. Other a-IGZO reports [12] account only 153.6 kHz. The LTPS based one [13] reported operation frequency is 20 kHz. This proposed circuits well function at 250 kHz which is sufficient to drive high-resolution 4K displays.

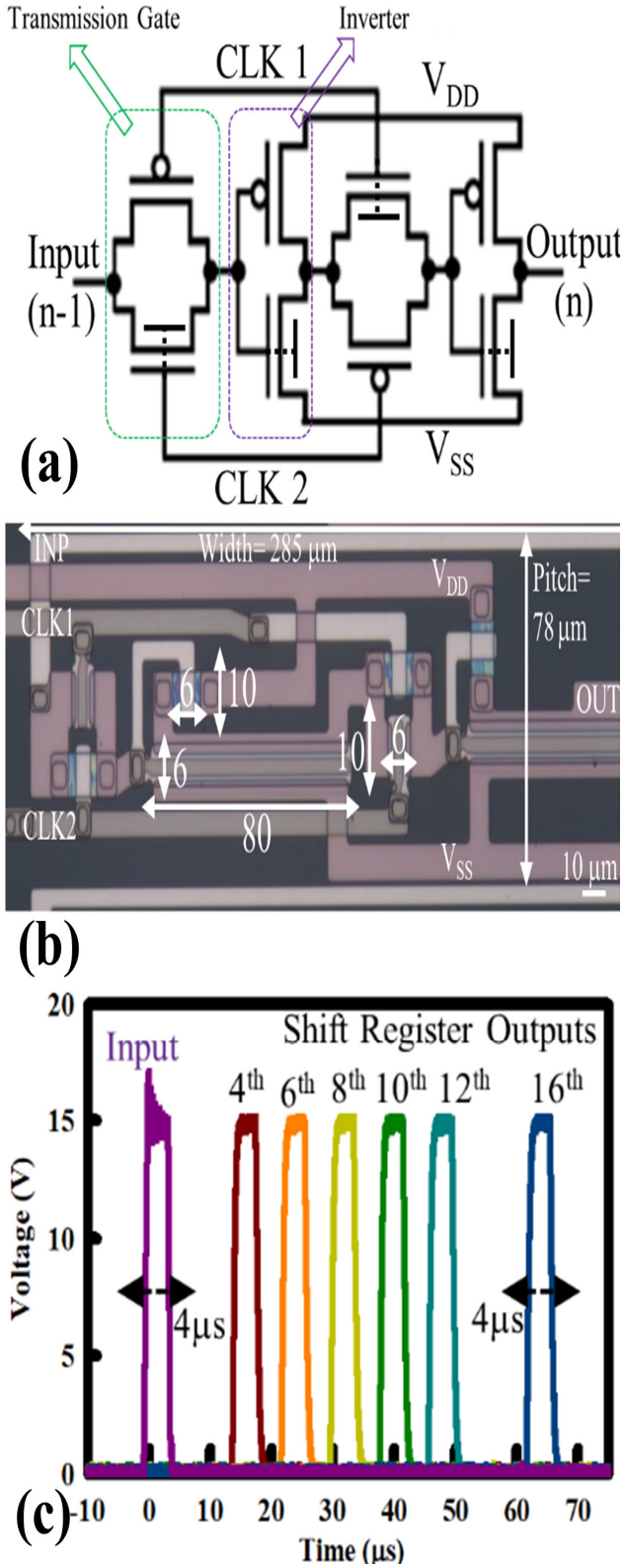

Figure 4. Conventional CMOS 2-clock shift register's single- stage TFT structured diagram (a), and the optical image (b). Measured output response of the shift register (SR) at the different stages are plotted in (c) for a 4 µs, 15 V input pulse.

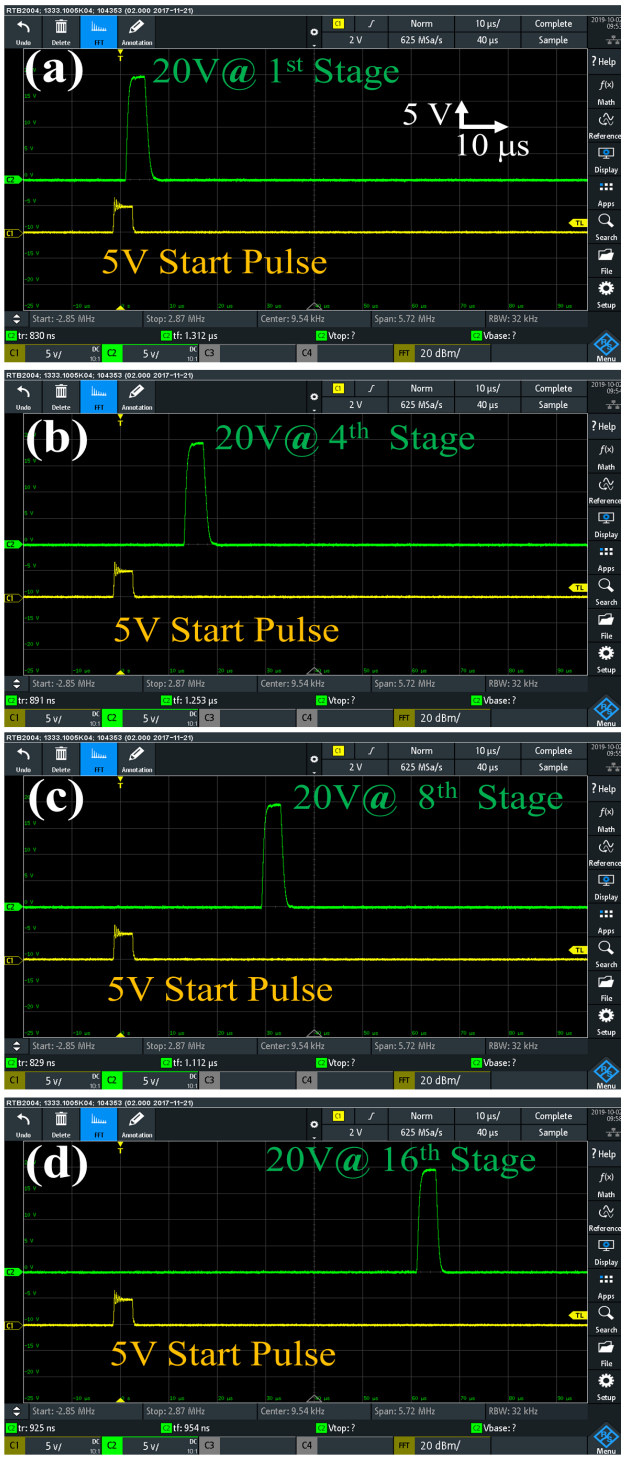

Figure 5. LTPO CMOS level shifter integrated gate driver measured performance for the operation frequency of 250 kHz. For a low 5V start pulse to the high 20V output, driving is shown for the 1st stage (a), 4th stage (b), 8th stage (c), and 16th stage (d).

4. Impact

We report the level shifter integrated gate drive circuits with LTPO TFT technology for the first time. The circuits well function in all stages and a low to high gate driving is demonstrated. Speed compatibility ensures it an attractive choice to drive AMOLED/UHD 4K displays in the near future.

5. Acknowledgments

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