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ANNEALING BEHAVIOR OF METASTABLE DEFECTS CREATED BY BIAS STRESS IN HYDROGENATED AMORPHOUS SILICON THIN FILM TRANSISTORS

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We have studied the annealing behavior of the metastable defects created by bias stresses in hydrogenated amorphous silicon thin film transistors. It is found that the annealing temperature of the created defects by bias stress depends on the sign of the gate bias voltage. The created defects by hole accumulation can be more easily removed by thermal annealing compared with the dangling bonds generated by a positive gate bias.

THERE IS A considerable interest in the application of hydrogenated amorphous silicon (*a*-Si : H) film to the fabrications of the thin film transistors (TFTs) for use in active matrix liquid crystal displays (LCDs), printer heads, image scanner, and image processing [1]. The *a*-Si : H films are mostly fabricated by a glow discharge technique, i.e., a conventional plasma enhanced chemical vapor deposition (PECVD).

The metastabilities in *a*-Si : H, arising from various external influences such as light illumination [2], current injection [3] and thermal quenching [4, 5], have been intensively studied in view of both fundamental physics and device applications. It is believed that the dangling bonds are created by light illumination [6] or by bias stress [7] in *a*-Si : H TFTs. In particular, the density of states around the midgap increases after positive or negative bias stresses [8]. The positive or negative bias stress gives rise to the increase in state density in the lower and upper half band gap region of *a*-Si : H respectively, confirmed by the measurements of the subthreshold swing before and after bias stresses [9]. There is a greater advantage in *a*-Si : H TFTs over films, since different defects can be generated when Fermi level is moved by gate bias without the presence of dopant atoms. In a recent paper Bae *et al.* [10] proposed a method to distinguish the different defect state through isochronal annealing in *a*-Si : H TFTs. In the present work, the isochronal annealing behavior of the created dangling bonds in positive or the negative bias stressed *a*-Si : H TFTs has been studied.

The transistors used in this study, have a conventional inverted staggered configuration. After the deposition and patterning of the Cr metal on Corning 7059 glass plates to make gate electrodes, three layers of silicon nitride (SiN), *a*-Si : H, and n^+ *a*-Si : H were deposited consecutively, in a separate chamber plasma chemical vapor deposition system. The deposition temperatures of the three layers were 350, 275, and 275°C, respectively. After making aluminum source/drain electrodes, the n^+ *a*-Si region between the source/drain electrodes was etched by reactive ion etching using a mixture of CF_4 and O_2. Then, the samples were heated at 200°C for 1 h to remove the residual metastable defects and the surface adsorbates. This is the annealed state. After prolonged application of a gate voltage, the drain currents were measured at a fixed temperature of 40°C. The threshold voltage was obtained from the extrapolation of a linear region of the transfer characteristics. Isochronal annealing temperature was increased up to 200°C in a step of 10°C under

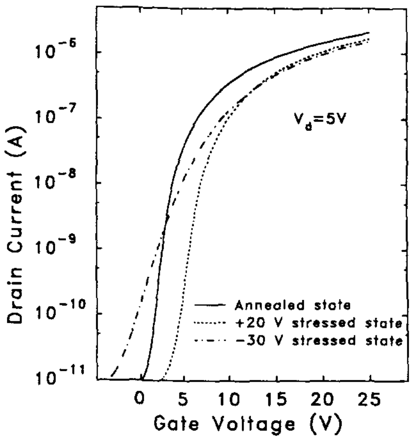

Fig. 1. The effect of bias stress on the transfer characteristics of *a*-Si : H TFT. The bias stresses were done at 40°C for 5 h.

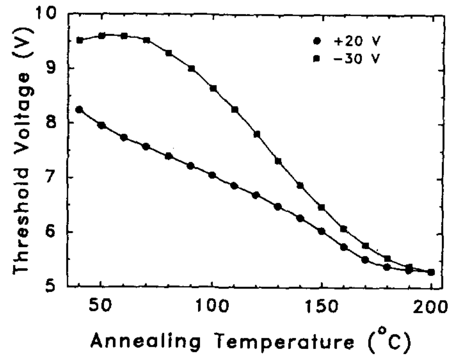

Fig. 3. The dependence of threshold voltage on the isochronal annealing temperature.

zero bias, and annealing time was fixed for 1 h at each temperature. Final annealing at 200°C for 1 h restored the initial transfer characteristics of annealed state.

Figure 1 shows the change in transfer characteristics by the various bias stresses. We can see a nearly parallel shift to the positive direction by a positive gate bias stress (electron accumulation) and an increase in the subthreshold slope by a negative bias stress (hole accumulation). The parallel shift of the threshold voltage means a creation of states in the gap in the lower half of the band gap, and the increase of the subthreshold swing indicates the creation of defects in the upper half of the band gap. This behavior is consistent with the results reported by Powell [9]. To obtain the threshold voltage (V_{th}), we plot the drain current vs gate voltage characteristics in linear scale. The results are shown in Figure 2. The threshold voltage shifts

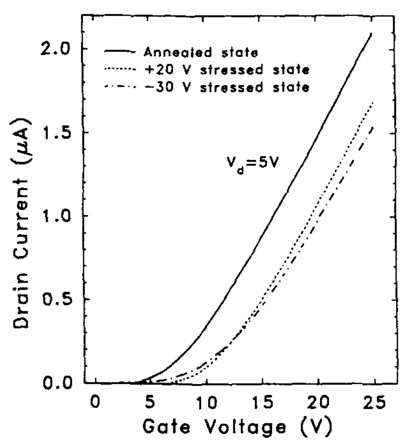

Fig. 2. The effect of bias stress on the transfer characteristics in linear scale. The threshold voltage is obtained from the linear region.

toward the positive direction for both positive and negative bias stresses for drain current in the range of μA.

The shift of threshold voltage by bias stress has also been reported by others [9, 11]. However, in contrast to our results, they observed a negative threshold voltage shift by negative bias stress, and Gelatos and Kanicki [11] noted that this result is induced by the hole trapping in the gate insulator.

Further experiments on the temperature and time dependence of threshold voltage shift by bias stress are performed. The results are similar to others [9, 11], but some results for negative bias stress are different. For negative bias stress, the positive shift of threshold voltage increases more rapidly, and saturation is observed at 40°C about several hours. This is consistent with the result that the light induced changes in the photoconductivity for boron doped sample are much faster than for the undoped sample [12] and p–i–p structures degrade at a significantly faster rate than n–i–n structures [3]. Therefore we can confirm that positive threshold voltage shift irrespective of the sign of gate bias stress voltage in our TFTs mainly is caused by defect creation in *a*-Si : H.

Figure 3 shows the annealing temperature dependencies of the V_{th}. As the annealing temperature increases, the V_{th} decreases until reaching an initial value.

Figure 4 shows the derivative of the threshold voltage with annealing temperature. We can expect an annealing behavior of the created defects from the derivative of the threshold voltage. For the positive bias of 20 V, the peak appears at 155°C. In contrast to the preceding result [10], the peak around 100°C associated with the annealing of interface defects is suppressed. This can be understood by the fact that the contamination of nitrogen in the channel region is reduced by an improvement of the gate insulator and interface. The derivative decreases gradually with an

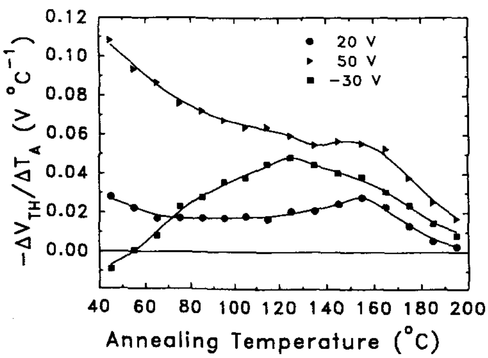

Fig. 4. The derivative of the threshold voltage with the annealing temperature.

increase in the annealing temperature for 50 V bias stressed TFT, but a peak appears at 155°C. It is believed that the trapping of charges into the silicon nitride becomes dominant as the gate voltage increases [13]. Therefore, the decreasing part in the 50 V bias case is probably due to the detrapping of the electron from the silicon nitride. The derivative for the negative bias case of −30 V increases with increasing annealing temperature, peaking at 125°C, indicating that the annealing of the defects is dominant rather than the detrapping of the holes from the silicon nitride. It is presumed that the hole trapping effect is not dominant in the case of −30 V bias stress, since the V_{th} decreases with increasing the annealing temperature as shown in Fig. 3. The detrapping of holes shifts the V_{th} toward the negative direction.

From our experimental results, it is concluded that the metastable defects created by a negative bias stress can be easily removed by thermal annealing compared with those created by positive bias stress. We can speculate that the difference in annealing temperature is related with the energy of the defects created by bias stresses. The positive bias stress increases the defects (D^-) in the lower half of the band gap, while the negative bias stress makes the defects (D^+) in the upper half of the band gap [9].

The microscopic picture to explain the difference in annealing temperature is not clear. However, a general comment is possible. The electron accumulation or hole accumulation near the interface can break the weak bonds and generates the dangling bonds. In this process, the diffusion of hydrogen atoms may act in an important role. We can speculate that the defect created by the trapping of excess electrons in weak bonds and by the deficit of electrons in weak bonds may have a different microscopic environment and correspondingly different annealing activation energy. Our work indicates that the annealing activation energy is lower for the defects created by a negative bias stress compared with those defects generated by positive bias stress. More detailed work should be done to clarify the microscopic picture of the created dangling bonds.

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