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A CMOS two-way time interleaved 12-bit SAR ADC with 6-bit MSBs sharing technique

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Abstract

This paper describes a two-way time interleaved 12-bit SAR ADC with 6-bit MSBs sharing technique. The proposed 12-bit SAR ADC consists of two SAR ADCs connected in parallel, so that the sampling rate can be doubled. The first 12-bit SAR ADC is employed to determine the 12 bits and the second 12-bit SAR ADC utilizes the upper 6-bits of the first one, so that it can determine the lower 6-bits and save switching energy. The proposed two-way time interleaved 12-bit SAR ADC is implemented with a CMOS 180 nm 1-poly 6-metal process. The measurement results demonstrate ENOB of 10.2 bits, SNDR of 62.9 dB, power consumption of 69 μW, INL/DNL of ± 1.8 LSB, and Walden FoM of 5.9 fJ/step.

Keywords CMOS · SAR ADC · Two-way time interleaved · Switching energy · 6-bit MSB sharing technique

1 Introduction

IoT (Internet on Things) with power efficiency has been rapidly developed to process a large amount of data from various sensors [1–4]. This drew attention to SAR (Successive Approximation Register) ADCs (Analog to Digital converter) which can provide not only a high resolution, but a high power efficiency. These SAR ADCs only suffer from low data conversion rate. Recently in order to resolve this problem, three design techniques have been proposed, including two-bits per step technique [5–7], four-way time interleaved technique [8], and two-way time interleaved technique [9].

Two-bits per step technique [5–7] allows SAR ADCs to convert data two times faster than the single bit per step SAR ADCs. However, it demands three comparators and six C-DACs (Capacitor-DAC) for differential signal processing, which consumes three times larger switching energy, compared to that of the conventional SAR ADC. Four-way time interleaved SAR ADC employs four SAR ADCs in the conventional time-interleaved way, so that it requires large switching energy due to C-DACs [8–10]. The conventional asynchronous two-way time-interleaved ADC technique used two identical 12-bit ADCs with one assistant 6-bit ADC. As the two main 12-bit ADCs convert data, the assistant 6-bit ADC provided the 6-bit MSB to the two main 12-bit ADCs in the time-interleaved way. Since the conventional technique employed three ADCs (two main 12-bit ADCs and one assistant 6-bit ADC), it suffered from a relatively large power consumption [9].

In this paper, the two-way time-interleaved SAR ADC with 6-bit MSB sharing technique is proposed not only to speed up the data sampling rate, but to reduce the switching energy. The proposed technique employs one main 12-bit SAR ADC and one assistant 12-bit SAR ADC. The assistant 12-bit SAR ADC receives the upper 6-bit directly from the main ADC, so that it only determines the lower 6-bit. This two-way time-interleaved technique allows the assistant ADC to employ only C-DAC for the lower 6-bit and to reduce switching energy of the assistant ADC.

This paper is organized as following: Sect. 2 describes the architecture and functionality of the proposed ADC. Section 3 presents the measurement results of the proposed ADC. Conclusions are drawn in Sect. 4.

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2 The proposed architecture

The block diagram of the proposed two-way time interleaved 12-bit SAR ADC with 6-bit MSBs (Most Significant Bit) sharing technique is presented in Fig. 1.

The proposed SAR ADC consists of a main 12-bit SAR ADC, an assistant 12-bit SAR, and a 12-bit output register to generate the final 12-bit binary code. The main 12-bit SAR ADC (ADC1) is composed of a preamplifier to block the kick-back noise of the clock signal, a latched comparator to generate data that will be fed to the 12-bit SAR logic, a 12-bit control logic to assist the 12-bit SAR logic, and two 12-bit C-DACs (Capacitor-Digital-to-Analog Converter) with the 64C/63 split capacitor to be controlled by the 12-bit SAR logic. The assistant 12-bit SAR ADC (ADC2) consists of the same architecture as the main ADC, except the 6-bit SAR logic and 6-bit control logic to control the 6-bit LSB (Least Significant Bit) switches of the 12-bit C-DAC. Since the 6-bit MSB switches of ADC2 shown in the shaded area in Fig. 1 are controlled by the 6-bit MSB of ADC1, the 36 differential switches of C-DAC in the ADC2 can be eliminated with respect to those of C-DAC in the ADC1. Elimination of 36 differential switches results in reduction of more than 50% switching energy of the proposed ADC with respect to the conventional ones. In order to maintain the linearity of the proposed ADC due to the inaccuracy of the split capacitor (64C/63), the MSB and MSB-1 capacitors in C-DAC of ADC1 and ADC2 are implemented by two identical capacitors connected in parallel through the common centroid layout technique. This design technique to divide one capacitor into two one-half capacitors in parallel resulted in enhancing not only the linearity, but the charging/discharging speed of the C-DACs. Enhancement of the charging/discharging speed of the C-DACs is also made by reducing the size of the switches associated with MSB and MSB-1 capacitors to one half [11]. Figure 2 illustrates the timing diagram of the clock, reset 1, reset 2, Q1, and 12-bits.

The reset 1 signal with a time period of every 14 clocks generated by the reset generator shown in Fig. 1 is to discharge all the capacitors in C-DAC of ADC1 and to sample the input signal. The Q1 signal produced by the 12-bit SAR logic circuit is to shift the 6-bit MSB determined by the ADC2 into the 6-bit MSBs of C-DAC of ADC2. The reset 2 signal with a time period of every 12 clocks is to discharge the capacitors associated with 6-bit LSBs of ADC2 and to sample the input signal. The reset 2 signal also allows the ADC2 to start determining the 6-bit LSB. The 12-bits determined by both ADC1 and ADC2 are shifted into the output register to deliver the final 12-bit binary codes in the two-way time-interleaved architecture. This operation is again illustrated by Fig. 3.

As the reset 1 signal (S1) is applied to ADC1, the ADC1 resets al1 the capacitors of C-DAC to discharge the residual charges and starts to determine 12-bits, and delivers the final 12-bits to the output register until the next S1 signal becomes high. As the reset 2 signal (S2) becomes high, the 6-bits MSBs already determined by ADC1 are shifted into the 6-bits MSB shift registers of ADC2. Hence the switching energy of the 6-bit MSB switches is saved because of the 6-bits MSB already determined by the ADC1. Finally, the 12-bits of ADC2 determined consequently are shifted into the output register to deliver the final 12-bit binary codes. Circuit diagram of the reset generator is presented in Fig. 4.

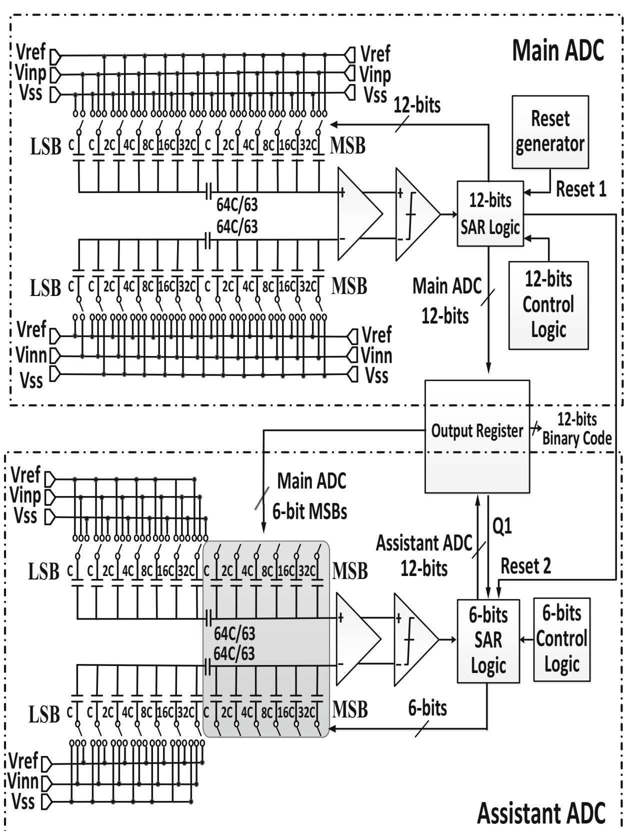

Fig. 1 Block diagram of the proposed SAR ADC

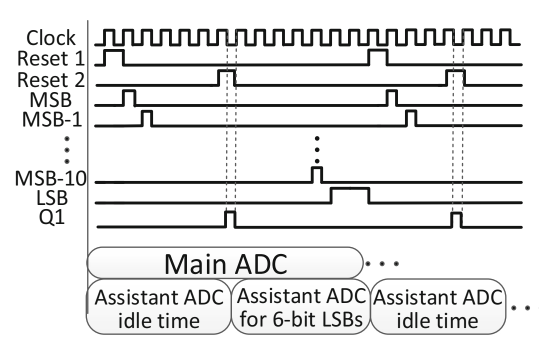

Fig. 2 Timing diagram of the proposed SAR ADC

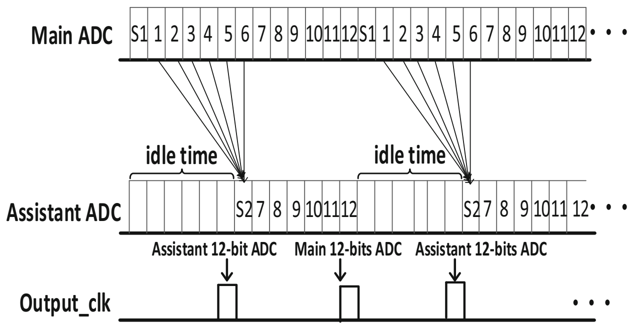

Fig. 3 Diagram of the two-way time-interleaved operation

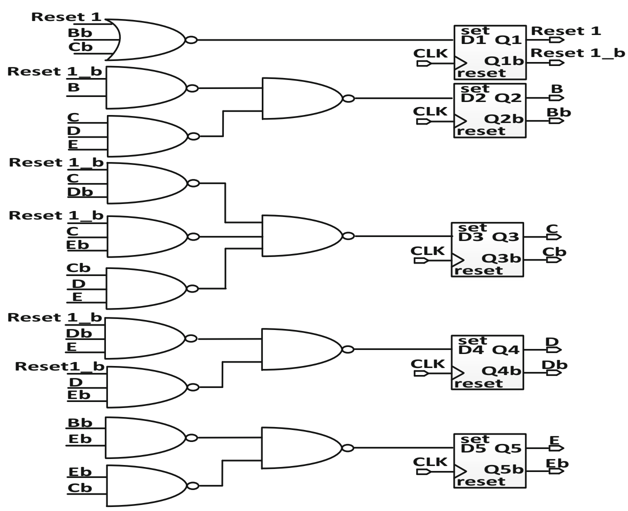

Fig. 4 Circuit diagram of the reset generator

Since the high signal of the reset 1 signal should be generated periodically every 14 clocks, Table 1 is utilized

Table 1 Table of reset generator

No	Reset 1 (R1)	B	C	D	E
1	0	0	0	0	0
2	0	0	0	0	1
3	0	0	0	1	0
4	0	0	0	1	1
5	0	0	1	0	0
6	0	0	1	0	1
7	0	0	1	1	0
8	0	0	1	1	1
9	0	1	0	0	0
10	0	1	0	0	1
11	0	1	0	1	0
12	0	1	0	1	1
13	0	1	1	0	0
14	1	1	1	0	0

as a truth table to derive (1) and to implement the circuit diagram of the reset generator through the Karnaugh map, as shown in Fig. 4.

$$\begin{aligned}
D1 &= \overline{R1}\, B\, C \\
D2 &= \overline{R1}\, B + CDE \\
D3 &= \overline{R1}C\bar{D} + \overline{R1}\, C\bar{E} + \bar{C}DE \\
D4 &= \overline{R1}\bar{D}\, E + \overline{R1}D\bar{E} \\
D5 &= \overline{BE} + \overline{EC},
\end{aligned} \tag{1}$$

where D1, D2, D3, D4, and D5 are the output signals of the D-flip-flops and R1 represents the reset signal 1.

The half circuit diagram of the differential C-DAC of the main SAR ADC (ADC1) is shown in Fig. 5.

Each capacitor within the C-DAC requires three switches based on transmission gate circuit, namely, the first one to sample input signal (V_{in}), the second one to connect to V_{ref} for "1" bit, and the third one to connect to V_{ss} for "0" bit. Total number of switches around the split capacitor is 40 switches, including one switch for V_{CM}, 21 (3 × 7) switches on the left hand side of the split capacitor, and 18 (3 × 6) switches on the right hand side of the split capacitor. Since ADC1 employs the differential C-DAC, the differential C-DAC of ADC1 employs 80 (3 × 7 × 2 + 3 × 6 × 2 + 1 × 2) switches. The half circuit diagram of the differential C-DAC of the assistant SAR ADC (ADC2) is shown in Fig. 6. Each capacitor of the C-DAC located at the left hand side of the split capacitor requires three switches, just like the same as the ADC1. However, each capacitor located at the right hand side of the split capacitor only requires two switches because 6-bit MSBs of ADC2 are directly connected to those MSBs of ADC1. Therefore, the differential C-DAC of ADC2 employs 68 (3 × 7 × 2 + 2 × 6 × 2 + 1 × 2) switches. Hence, the total number of switches employed by the C-DACs of ADC1 and ADC2 is 168.

The switching energy, E_{con} consumed by the conventional C-DACs with a split capacitor is calculated to be 6,822C $V_{ref}^2 \times f_s$ [12, 13]. The switching energy of the assistant ADC (ADC2) proposed in this paper turns out to be 83C $V_{ref}^2 \times f_s$ because ADC2 only consumes the switching energy to determine the lower 6 bits. The total switching energy of the C-DAC of the proposed ADC is

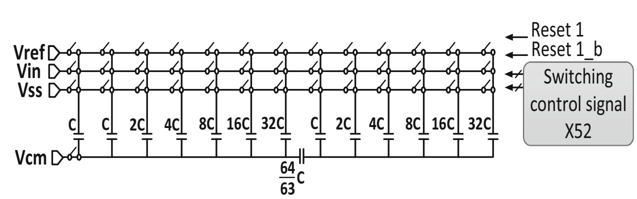

Fig. 5 The half circuit diagram of the differential C-DAC of the main ADC (ADC1)

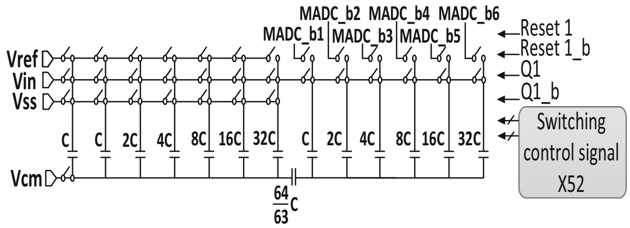

Fig. 6 The half circuit diagram of the differential C-DAC of the assistant ADC (ADC2)

calculated to be 3494C $V_{ref}^2 \times f_s$ because of adding 3411 $V_{ref}^2 \times f_s$ (ADC1) to 83C $V_{ref}^2 \times f_s$. Comparison of the normalized switching energy of two architectures with respect to the switching energy of the conventional architecture is made in Table 2. The normalized values of the switching energy are 1 and 0.51. Table 2 illustrates the switching energy of the proposed architecture is reduced down to 51% with respect to that of the conventional one.

3 Measurement results

The proposed two-way time-interleaved 12-bit SAR ADC with 6-bit MSBs sharing technique is implemented with a 180 nm CMOS 1-poly 6-metal process. Chip micro-photograph is illustrated in Fig. 7. Analog building blocks such as differential C-DACs, pre-amplifiers, comparators, and switch array are placed on the top of the chip to be isolated from the digital circuits. Digital building blocks are placed on the bottom of the die, including control logics, a reset generator, a shift register, 12-bits SAR logic, and a 12-bits output register. The main ADC (ADC1) and the assistant ADC (ADC2) occupy three quarters and one quarter of the total chip area, respectively. The effective core chip size excluding bonding pads is measured to be 600 um × 900 um.

The photograph of the test fixture with the proposed chip on the PCB is presented in Fig. 8. The digital 12 binary pins, digital power supply, and digital ground connectors are placed to be separated from the differential analog signal, analog power supply, and analog ground connectors. The clock signal (CLK), reference voltage, and digital common-mode voltage (DVCM) are provided by the low-jitter clock generator and the band gap reference circuit, respectively.

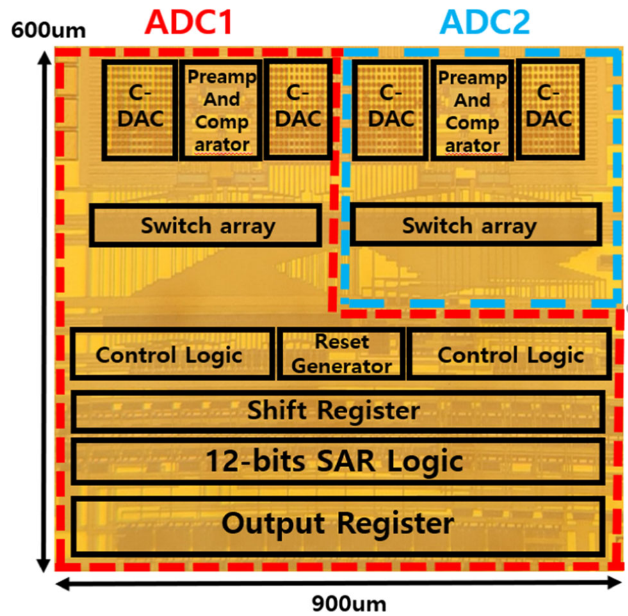

Fig. 7 Chip photograph of the proposed SAR ADC

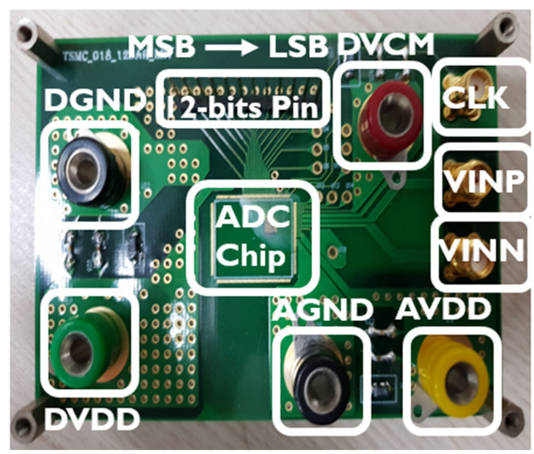

Fig. 8 Photograph of the test fixture with the proposed chip on the PCB

The reset 1 and reset 2 signals produced by the reset generator and 12-bit SAR logic circuit, respectively are measured, as shown in Fig. 9. The time period (2800 ns) of the reset 1 and reset 2 signals is exactly the same after every 14 clocks except the delay time of 6 clocks (1,200 ns). This measurement result proves the proper functionality of the reset generators and 12-bit SAR logic circuits, so that two signals allow ADC1 and ADC2 to be

Table 2 Comparison of the normalized switching energy of two architectures

Architecture	Conventional architecture	Proposed architecture
Switching energy/C V_{ref}^2 f_s	6822	3494
Normalization	1	0.51

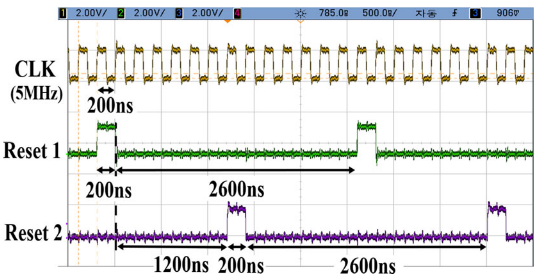

Fig. 9 The measured waveforms of the clock, reset 1, and reset 2 signals

able to produce 12-bits in the two-way time-interleaved architecture with the 6-bit MSBs sharing technique.

The DNL and INL of the proposed ADC are measured to be within ± 1.8 LSB, as shown in Fig. 10. This resulted from the design technique to divide one capacitor of MSB/MSB-1 of C-DAC into one half capacitors connected in parallel with the common centroid layout technique.

Total power consumption of the proposed chip is measured to be 69 µW, including analog power of 10 µW and digital power of 59 µW. Most of the digital power is consumed by the digital control logic circuits and output register. The measured FFT result at the input frequency of 1 kHz (sinusoidal wave) and clock frequency of 10 MHz demonstrates SINAD of 62.9 dB and ENOB of 10.2-bit, respectively, as shown in Fig. 11. It results in Walden FoM of 5.7 fJ/step. The equation of Walden FoM is given in (2).

$$FoM_{Walden} = \frac{Power\ consumption}{f_s \times 2^{ENOB}} \quad (2)$$

where f_s and ENOB are the Nyquist sampling frequency and effective number of bit, respectively.

Figure 12 illustrates the measured ENOB of 10.2-bits to 7.2-bits at the clock frequency of 10 MHz as a function of the input frequency of the sinusoidal waveform, ranging from 1 kHz to 400 kHz.

The maximum ENOB of 10.3-bits is measured below the clock frequency of 500 kHz with the fixed input frequency of 1 kHz, as shown in Fig. 13. Comparison of the performance of the proposed ADC with that of the conventional ones made in Table 3 shows that the performance of the proposed ADC is comparative to that of the others. Especially, the power consumption and Walden FoM of the proposed one achieved the minimum, comparing with others.

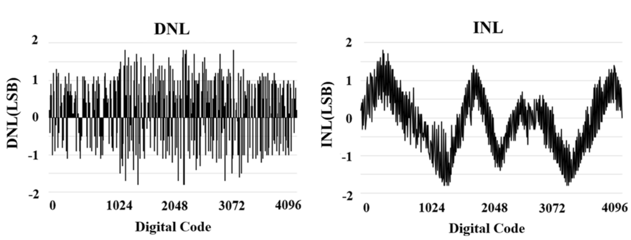

Fig. 10 The measured waveforms of the DNL and INL

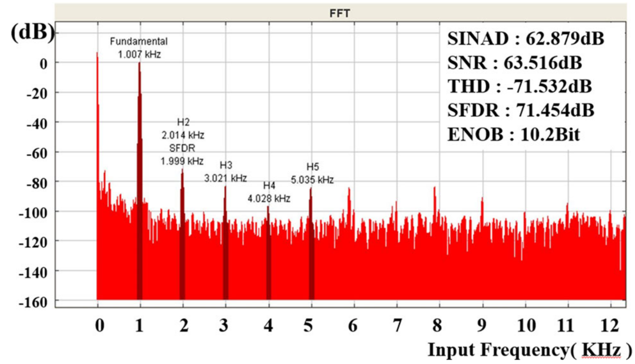

Fig. 11 The measured FFT result at the input and clock frequency of 1 kHz and 10 MHz, respectively

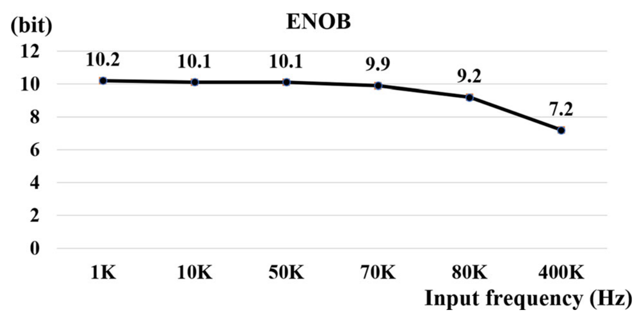

Fig. 12 The measured plot of ENOB as a function of the input frequency at the fixed clock frequency of 10 MHz

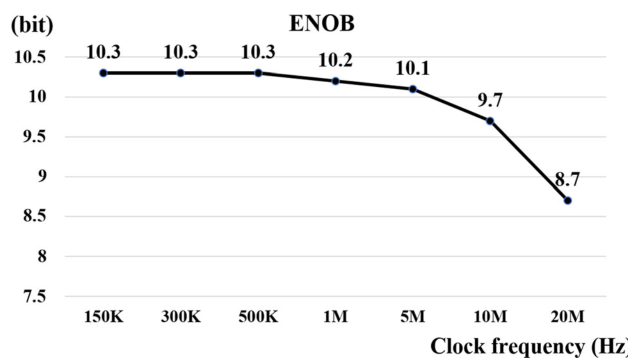

Fig. 13 The measured plot of ENOB as a function of the clock frequency at the fixed input frequency of 1 kHz

4 Conclusions

A 6-bit MSBs sharing technique for two-way time interleaved SAR ADC was proposed. The proposed technique allows the ADC to reduce both a number of switches in C-DACs and switching energy because of the 6-bit MSBs of the ADC1 sharing with those of the ADC2. The proposed ADC with 10 MS/s of clock achieved power

Table 3 Comparison of the performance of the proposed SAR A/D converter with conventional ones

Parameter	[5]	[6]	[7]	[8]	[9]	This work
Architecture	2-bit/step	2-bit/step	2-bit/step	Four-Way Interleaved	Two-Way Interleaved	Two-Way Interleaved
CMOS Process	65 nm	180 nm	28 nm	40 nm	65 nm	180 nm
Resolution	10	10	7	10	12	12
Supply voltage (V)	1.1	1.8	0.9	1.1	0.6	1.8
Speed	400 MS/s	100 MS/s	2.4 GS/s	800 MS/s	10 MS/s	10 MS/s
SNDR (dB)	51.9	52.3	40.05	48	65	62.9
ENOB (bit)	8.3	8.4	6.3	7.7	10.5	10.2
Power consumption	5.6 mW	6.5 mW	5 mW	4.9 mW	83 µW	69 µW
Walden FoM	43 fJ/step	191 fJ/step	25.3 fJ/step	28.8 fJ/step	6.2 fJ/step	5.9 fJ/step

consumption of 69 µW, DNL/INL of ± 1.8 LSB, ENOB of 10.2-bit, and Walden FoM of 5.9 fJ/step. The measurement results demonstrated the switching energy efficiency of the 6-bit MSBs sharing technique of the proposed SAR ADC in terms of the power consumption and Walden FoM. It is expected that if a multi-bit MSBs sharing technique is applied to design multi-way time interleaved SAR ADC, it will enhance the switching energy efficiency of high resolution and high speed SAR ADC without sacrificing dynamic performance.

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