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RESEARCH ARTICLE

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Enhancing stretchable display performance: IGZO TFT pixel circuit with luminance compensation

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Abstract

Despite the flexible form factor advantages of stretchable organic light-emitting diode displays, their luminance diminishes as the area expands. In this study, we introduced and assessed a novel pixel circuit aimed at efficiently compensating for luminance changes resulting from the stretching of the display area. The proposed pixel circuit incorporates a sensing capacitor for compensation, enhancing pixel current to counteract luminance reduction when the pixel expands through stretching. The sensor capacitor's capacitances align with the stretched area, resulting in a 16.9% increase in pixel current with a 10% capacitance rise and a 24.1% increase with a 20% capacitance increase. This observation serves as evidence of the circuit's successful compensation for stretching. Additionally, the proposed pixel circuit can reduce both data and power voltages compared to the conventional one. Consequently, the proposed pixel circuit offers lower power consumption compared to the conventional one.

KEYWORDS

compensation, luminance, organic light-emitting diode (AMOLED), pixel circuit, stretchable display

1 | INTRODUCTION

As the demand for durable, ultraightweight, foam-changeable displays increases, research has been conducted to implement flexible displays and electronics using flexible substrates.[1–5] Stretchable displays are considered the most advanced form of flexible displays allowing for free form designs unrestricted by shape alterations.

Amorphous indium-gallium-zinc-oxide (a-IGZO), a semiconductor material employed in thin-film transistors (TFTs), has become a preferred choice for the backplane of large-size display panels. This selection is attributed to its advantageous features, including high field-effect mobility and low leakage current compared to amorphous silicon TFTs and large-size processability.[6–8] Given these advantages, the utilization of a-IGZO-based TFTs has been under investigation for integration into flexible display technologies.[9–12]

Active-matrix organic emitting diode (AMOLED) displays, one of the most attractive displays for stretchable displays, have been applied to various products, such as mobile phones and television, based on advantages, such as high contrast, rapid response time, and wide viewing angle, compared to liquid crystal displays. In addition, AMOLEDs have a relatively high physical deformation degree of freedom compared to other display technologies and have been studied for various types of flexible displays, including stretchable displays.[13–18] For example, Hong et al. produced a 9.1-in. stretchable AMOLED that could form a convex/concave shape on a PI substrate in 2017.[13] On the other hand, there is an issue with a luminance imbalance caused by the stretched area and

voltage drops in power lines. Because the AMOLED is a current-driven display, a voltage drop by the power line resistance causes a luminance imbalance due to current variations by voltage differences supplied to each pixel. Various studies have been conducted on pixel circuits to compensate for the luminance imbalance caused by the voltage drop.[19–22] In a stretchable display, the luminance in a stretched area decreases, which should be compensated to maintain the luminance under the stretching.

Because the TFT and OLED degrade under stretching, one strategy is to maintain hardness for those areas where devices are formed.[23–25] The island–bridge structure, the most representative structure to prevent the characteristic changes of the devices, places them on rigid areas of the island and wires on the stretchable area. The effect of the change in the device characteristics on the luminance and their compensation were studied in the stretchable display.[26–29] While compensation for stretching has been proposed, there has been no consideration for compensation for the threshold voltage shift in the TFT.[26] Kang et al. introduced a pixel circuit designed to compensate for the threshold voltage variation in the drive TFT, ensuring consistent luminance, except for the compensation specifically targeted for stretching and voltage drop in the power lines.[27] A compensation pixel circuit, designed to counteract the strain-induced degradation of TFTs in a flexible display, was proposed. This approach involved the utilization of an inverter circuit for effective compensation.[28] Active compensation of OLED current becomes essential to counteract the reduced luminance resulting from the stretched area. This involves a necessary increase in OLED current specifically within the stretched region to facilitate effective compensation. In this study, we accomplished active compensation for stretching by autonomously increasing the OLED current during stretching. We have proposed and developed a pixel circuit that not only compensates for the reduction in luminance due to the stretched area but also provides low power consumption. The circuit's efficacy was validated through simulations and measurements.

2 | PROPOSED PIXEL CIRCUIT

To detect stretching, the sensor capacitor C2 has been incorporated into the pixel circuit, as illustrated in Figure 1A. The act of stretching the substrate leads to an increase in the capacitance of C2. The other parts are formed on a rigid area, which is a usual strategy to establish the stretchable display. Among several strategies to achieve a stretchable display, the rigid area islands are used to prevent changes in characteristics during compensation. TFTs and OLEDs are formed on the rigid areas, while stretching occurs only in the elastomeric regions. This design prevents changes in the characteristics of the devices during compensation by isolating the rigid areas from the deformation. The sensor capacitor C2 is formed on a stretching area. The change of the capacitances by stretched area is reported and can be used for the sensing of the stretching.[29,30] Figure 1B illustrates the driving scheme. The voltage levels, transistor sizes, and capacitance values we used are detailed in Table 1.

Figure 1A,B show the proposed pixel circuit with its driving scheme. The circuit consists of three n-channel switching TFTs (T1, T3, and T4), an n-channel drive TFT (T2), one storage capacitor (C1) in the rigid area, and one stretchable capacitor (C2) in the soft area. T1 is a row selection switch that stores the data voltage in the gate (Node P) of T2 and C1. T3 and T4 control the voltages applied to Node Q, where the change in luminance in the

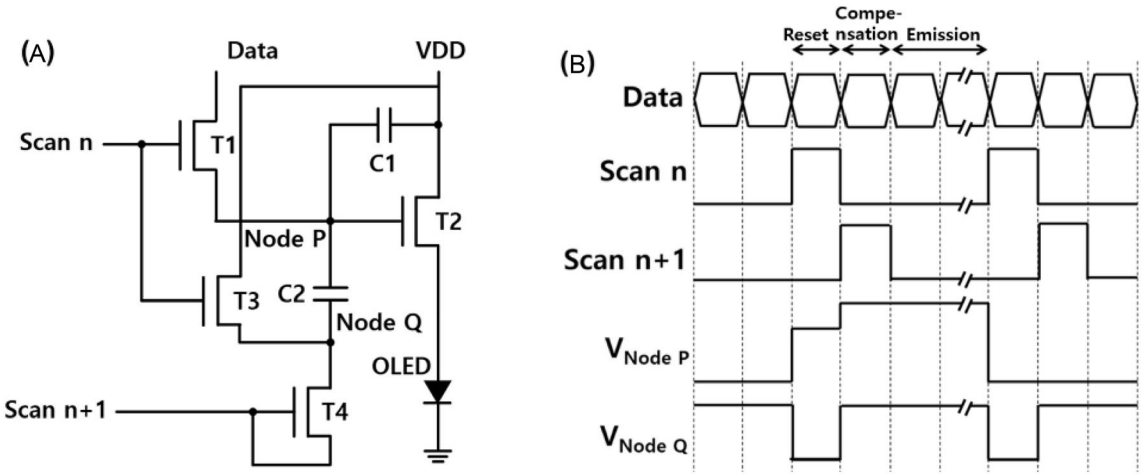


FIGURE 1 (A) Proposed pixel circuit and (B) its driving scheme.

TABLE 1 Parameters used in the simulation.

Parameters	Value
VDD (V)	7
Scan (V)	−5–10
Data (V)	0–4
T1, 3, 4 W/L (μm)	20/10
T2 W/L (μm)	40/10
Capacitance of C1 (pF)	0.3

stretched area is compensated for by utilizing the change in capacitance of the C2. The capacitance of C2 depends on the stretched area in a pixel.

The initial phase of the compensation process is the reset stage, which involves charging nodes P and Q. As shown in Figure 1B, this occurs when Scan (n) reaches a high voltage, activating transistors T1 and T3. As the T1 and T3 are turned on, the voltages in the V_{NodeP} and V_{NodeQ} become a data voltage and V_{DD}, respectively. In this case, the voltages of each Node are as follows.

$$\begin{aligned} V_{NodeP} &= V_{Data} \\ V_{NodeQ} &= V_{DD} \end{aligned}, \tag{1}$$

To facilitate this operation, the high voltage of the scan pulse must surpass the V_{DD} level.

The next compensation phase begins when Scan(n + 1) goes high. T4 acts as a forward-biased diode when Scan (n + 1) becomes high. Since the high voltage of the scan pulse exceeds V_{DD} by a margin greater than the threshold voltage, V_{NodeQ} transitions from V_{DD} to $V_{Scan} - V_{T4}$, when Scan (n + 1) becomes high. V_{T4} is the threshold voltage of T4. Therefore, the voltage change at node Q is $V_{Scan} - V_{T4} - V_{DD}$. As V_{NodeQ} raises from V_{DD} to $V_{Scan} - V_{T4}$, there is a consequential change in V_{NodeP} due to the floating state of Node P. Given that the parasitic capacitances of T1 and T2 are considerably smaller than C1, the voltage at Node P is influenced by the C2 to C1 ratio. The V_{NodeP} follows the principles of simple charge conservation, during change of the NodeQ voltages from V_{DD} to $V_{Scan} - V_{T4}$. Therefore, the voltage at Node P is changed from V_{Data} to

$$V_{NodeP} = V_{Data} + \frac{C2}{C1+C2}(V_{Scan} - V_{T4} - V_{DD}). \tag{2}$$

Given that V_{DD} consistently remains lower than the scan voltage in this circuit, Equation (2) indicates that V_{NodeP} surpasses V_{data} as V_{NodeQ} increases. When a voltage drop occurs in the V_{DD} line of a pixel due to IR drop, the voltage applied to the drive TFT decreases, leading to a reduction in V_{DD} in Equation (2). Consequently, V_{NodeP} increases as per Equation (2). This rise in V_{NodeP} acts as a compensatory measure for the decrease in current resulting from the voltage drop in the V_{DD} line. In scenarios involving stretching, the capacitance of C2 experiences an increase. Consequently, V_{NodeP} rises by Equation (2) due to the increased capacitance of C2. The elevation of V_{NodeP} leads to an increase in the currents flowing through the OLED, effectively compensating for the decreased luminance in the stretched area.

During the emission period, T2 is activated by V_{NodeP}, enabling the compensated current to flow through the OLED. The OLED current (I_{OLED}) establishes the voltage across both ends of the OLED. Given that the gate-source voltage (V_{GS}) of T2 is determined by $V_{NodeP} - V_{OLED}$, the expression for I_{OLED} is as follows.

$$\begin{aligned} I_{OLED} &= \frac{k}{2}(V_{GS} - V_{T2})^2 \\ &= \frac{k}{2}\left[V_{Data} + \frac{C2}{C1+C2}(V_{Scan} - V_{T4} - V_{DD}) - V_{OLED} - V_{T2})\right]^2. \end{aligned} \tag{3}$$

where k is $\mu \cdot C_{OX} \cdot W/L$ in which μ is the field-effect mobility, C_{OX} is gate insulator capacitance per unit area, W channel width, L channel length, and V_{OLED} the source voltage of T2. Following Equation (3), the OLED currents exhibit an increase due to both the reduced V_{DD} and the increased capacitance of C2. This compensatory mechanism efficiently reduces luminance fluctuations caused by both voltage drop and area stretching. In Equation (3), I_{OLED} is influenced by the threshold voltages of T2 and T4, suggesting an area for potential improvement through further research.

3 | EXPERIMENT

Top gate a-IGZO TFT was used in this circuit as shown in Figure 2, where the gate insulator and interlayer dielectric were negative photoresistors of SU8.

FIGURE 2 The schematic cross-sectional structure of a fabricated amorphous indium-gallium-zinc-oxide (a-IGZO) thin-film transistor (TFT).

After cleaning a glass substrate, an a-IGZO with a thickness of 500 Å was deposited by RF magnetron sputtering at gas flows of Ar: 22.5 sccm and O_2: 7.5 sccm using a target with a mole ratio of In_2O_3: Ga_2O_3: ZnO = 2: 1: 2. Following the patterning of the active region, a 5000 Å thick SU-8 film was uniformly coated through the spin coating at 1000 RPM. Subsequently, a layer of aluminum, 2000 Å in thickness, was deposited using DC magnetron sputtering with an Ar gas flow of 20 sccm. Following the wet etching process for aluminum gate electrode fabrication, selective removal of the SU-8 film was achieved, leaving it only under the gate electrode through reactive ion etching with an O_2 gas flow of 60 sccm. After these steps, an oxygen plasma treatment was carried out to facilitate doping in the source and drain areas.

After applying a 5000 Å SU-8 layer as an interlayer dielectric, contact holes were formed to establish connections between the a-IGZO layer and the source/drain electrodes. Subsequently, Al source/drain electrodes were formed through the deposition of aluminum using DC magnetron sputtering. Figure 3 presents the microscopic view of the fabricated pixel circuit. The channel lengths of all TFTs were 10 μm. The channel width of T2 was 40 μm, and others were 20 μm. The area of the proposed pixel was 220 × 230 μm.

To validate the pixel circuit, we monitored the current flowing through the drive TFT. For the measurement of transient currents during pixel operation, scan pulses, data voltage, and V_{DD} were applied to the pixel. Subsequently, the current at the source electrode of the drive TFT was measured. An amplifier was employed to amplify the minute currents, and the output currents from the amplifier were routed to the ground through a resistor. The oscilloscope was utilized to monitor the transient currents by measuring the voltage across the resistor inserted between the current amplifier and the ground.

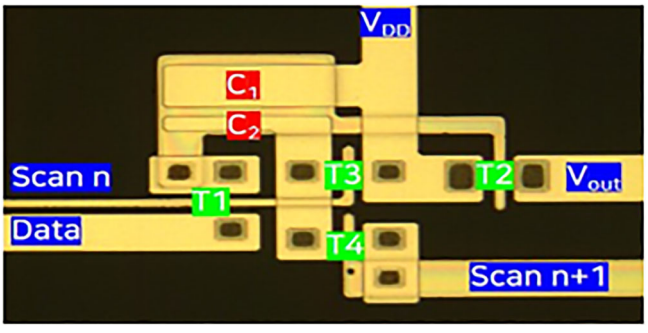


FIGURE 3 The microscopic view of the fabricated pixel circuit.

4 | RESULTS AND DISCUSSION

Figure 4 illustrates the transfer characteristics of the manufactured a-IGZO TFT, with channel dimensions set at 40 μm for width and 10 μm for length. The mobility and threshold voltage were 0.1 $cm^2/V{\cdot}s$ and 6.2 V, respectively. The I_{on}/I_{off} ratio was 3.0×10^7, and the subthreshold slope was 4.4 V/dec.

The observed low mobility and significant threshold voltage can be attributed to interface defects or imperfections in the SU-8 gate insulator. However, despite these challenges, circuit verification was successfully conducted using these TFTs. By applying input signals to the pixel, transient currents through T2 were measured to investigate the compensation mechanism of the circuit. For measuring small transient currents, we utilized a current amplifier, as depicted in Figure 5A,B.

Accurately measuring small currents with minimal noise presented a significant challenge. After undergoing a series of trial and error, we managed to successfully measure these delicate currents, marking a notable achievement for our study. Pixel currents are inherently low and thus susceptible to disturbances during measurement. To address this issues, we employed a Keithley 428 current amplifier, which effectively amplifies the input currents for more accurate monitoring. The amplified currents pass through a resistor, converting the current into a voltage signal that can be effectively monitored using an oscilloscope. This amplifier was specifically designed to interface with an oscilloscope or waveform digitizer to display extremely low currents in real-time. It features a rapid response at low current levels and offers a current voltage inverting output BNC

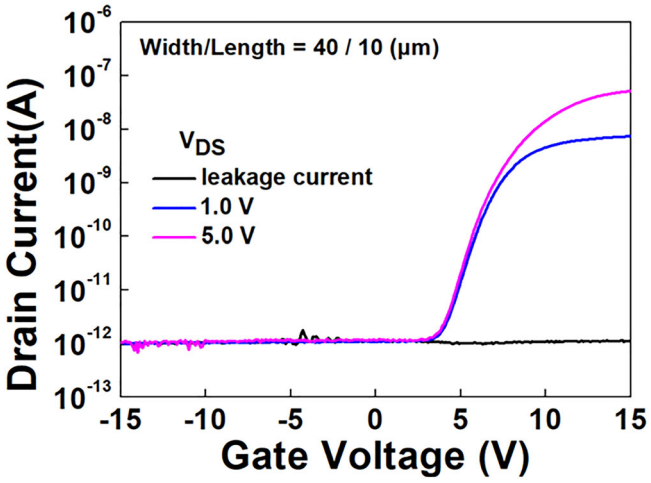
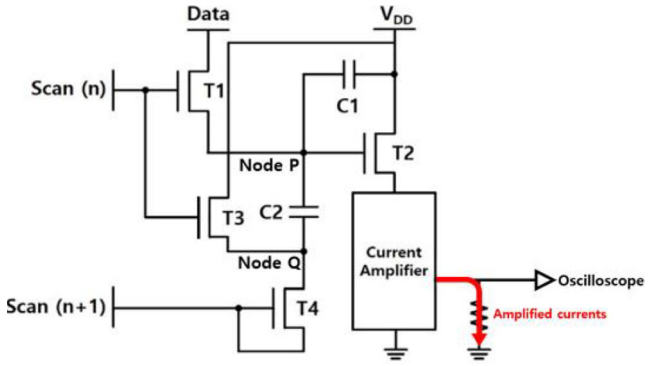
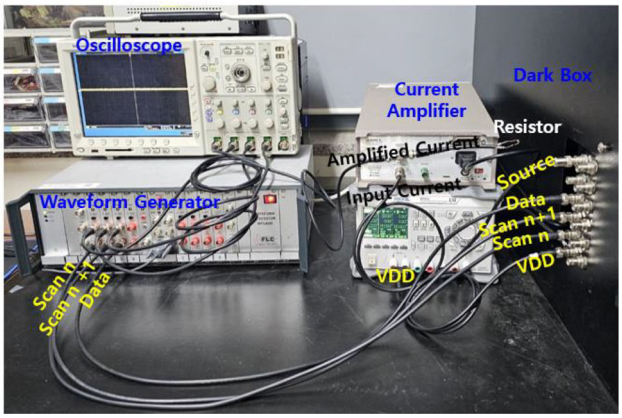


FIGURE 4 Transfer characteristics of the fabricated amorphous indium-gallium-zinc-oxide (a-IGZO) thin-film transistor (TFT).



(a)



(b)

FIGURE 5 (A) Schematic of the current measurement setup and (B) photograph of the measurement setup.

connection. This monitoring output voltage greatly simplified the measurement of transient low currents, thereby improving the accuracy of our analysis.

Figure 6 illustrates the data pulse (top), scan pulses (middle), and currents (bottom). Scan (n) and Scan (n + 1) were applied alternately, while the data voltages cycled between low and high states. We optimized the pulse width and voltages to achieve the most effective OLED operation. As shown in currents (bottom), the current increased owing to the elevated V_{NodeP} upon applying Scan (n) with a high data signal. Following this, upon the application of Scan (n + 1), V_{NodeP} increased even more as explained in Equation (2), leading to an amplified driving current as described in Equation (3).

The currents depicted in Figure 6 are greater than the measured currents in TFTs, as shown in Figure 4. We attribute the current difference to the nonuniform characteristics on a substrate and inadequate reliability of the TFTs, challenges that are difficult to take over within a university laboratory setting. Environmental factors within the laboratory, process nonuniformity, and the

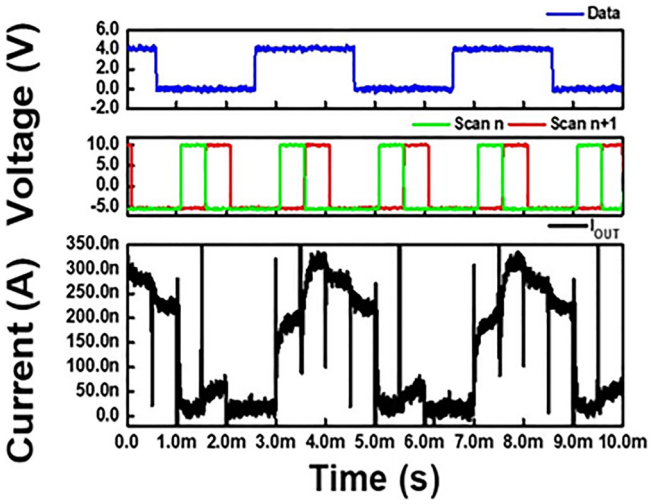


FIGURE 6 Data voltages (top), scan pulses (middle), and currents (bottom).

loading effect increase the nonuniformity of the TFT characteristics.

As illustrated in Figure 6, the currents exhibit an increase during Scan (n) under high data voltage and further escalate during Scan (n + 1) owing to the heightened V_{NodeP} as described in Equation (2). As C2 is situated on a stretchable area to facilitate compensation for stretching, three distinct pixel circuits were manufactured, each featuring a different capacitance of C2. This was done to validate the effectiveness of compensation for the area stretching. In an actual stretchable display, the capacitor is created using a stretchable dielectric material positioned between two electrodes or between two coplanar electrodes on an elastomer substrate. In general, stretching-induced strain can damage the capacitor, so special care is required to ensure it functions properly under varying levels of strain. The choice of electrodes is especially critical in stretchable capacitors. For example, a stretchable capacitor using silver nanowires/reduced graphene oxide (AgNWs/rGO) has been demonstrated on a PDMS substrate.[29] They demonstrated that capacitance increases with greater stretching. Stretching the capacitor can lead to increased leakage current or even breakage, particularly when using an inorganic insulator. To address these issues, a conductance-variable structure can be employed as a compensation strategy, using changes in conductance to adapt to the strain.[31]

Figure 7 and Table 2 depict the currents for each pixel circuit. The variation in C2 is reflected in distinct V_{NodeP} values, leading to differences in currents across the circuits. Throughout the charging stage, characterized by the high Scan (n), the currents for all three pixels with varying C2 exhibit similarity across the different circuit types. However, distinctions emerge during Scan (n + 1),

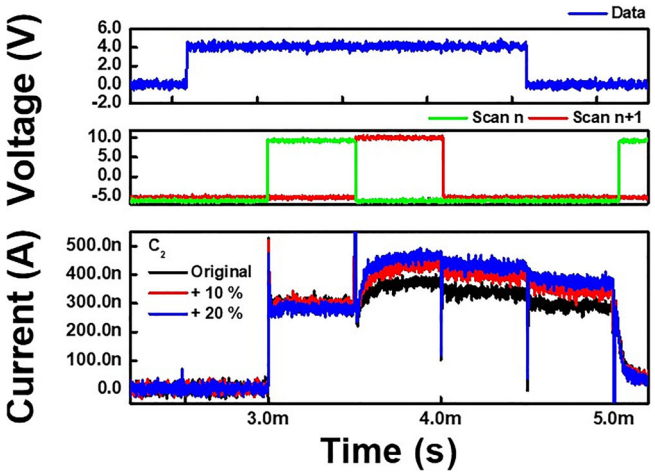


FIGURE 7 Measurement results of the three types of proposed pixel circuits.

TABLE 2 Pixel currents corresponding to different values of capacitance for C2.

Capacitances of C2	Measured currents	Increase
Ref. (0.10 pF)	378.1 nA	-
+10% (0.11 pF)	441.8 nA	16.9%
+20% (0.12 pF)	469.2 nA	24.1%

aligning with the predictions outlined in Equation (3). When the Scan n + 1 voltage drops from high to low, we observe small current drops attributed to the voltage decrease at Node P caused by the Scan n + 1 voltage drop. Similar drops occur when the data voltage decreases for the same reason. As the Scan n voltage increases again, the currents decrease due to the low data voltage, resulting in a dark current.

The pixel circuit's current with a C2 capacitance of 0.10 pF was 378.1 nA, while the measured current for the circuit with a C2 of 0.11 pF increased to 441.8 nA, indicating a 16.9% rise compared to the current with C1. Furthermore, the measured current for the pixel circuit with a C2 capacitance of 0.12 pF was 469.2 nA, representing a 24.1% increase compared to the circuit with a C2 of 0.10 pF. The currents in the pixel circuits demonstrated a consistent increase with the growing capacitance of C2, driven by the elevated V_{NodeP} as determined by Equation (2). As a result, the proposed pixel circuit demonstrates its ability to compensate for a decrease in luminance caused by an expanding area.

A conventional pixel circuit was manufactured for comparative purposes to validate the compensation capabilities of the proposed pixel circuit for voltage drop. Figure 8 displays the schematic, microscopic view, and measurement results of the circuit. The fabricated

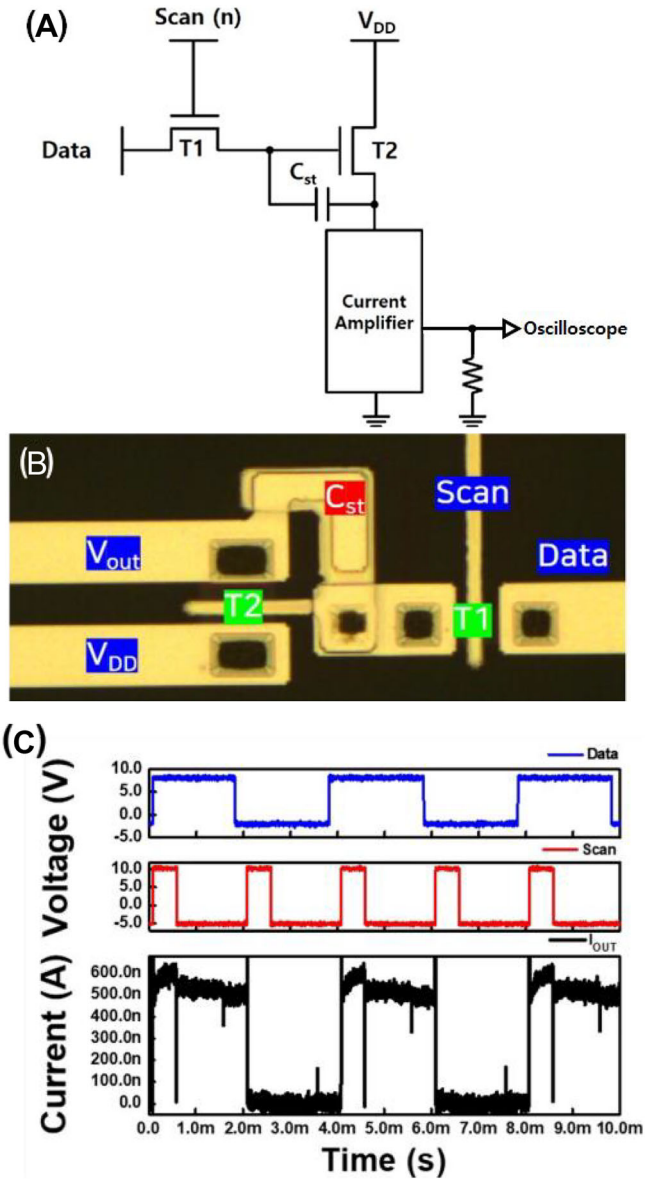


FIGURE 8 (A) The schematic diagram of the circuit (B) microscopic view and (C) measurements of the fabricated conventional pixel circuit.

conventional pixel circuit consisted of two a-IGZO TFTs and one capacitor. The channel lengths of the two TFTs were 10 μm, and the channel widths of T1 and T2 were 20 and 40 μm, respectively. The capacitance of the storage capacitor was designed to be 0.10 pF. The area of the conventional pixel circuit was 180 × 130 μm. The data voltages alternated between high and low, resulting in currents that followed the same pattern, corresponding to the fluctuating data voltages. This behavior is illustrated in Figure 8C. The decline in current during the descent of the scan pulses can be ascribed to the decrease in the gate voltage of T2. The voltage charged to the gate node of T2 experiences a sudden drop when the scan pulse

decreases to a low voltage, a phenomenon known as kickback or level shift. This voltage drop occurs due to the parasitic capacitance associated with the switch TFT T1. Consequently, a decrease in current is observed in accordance with the kickback, as depicted in Figure 8C. This precise measurement of current changes emphasizes the effectiveness and utility of the current amplifier.

Figure 9 and Table 3 illustrate the current variations in both the conventional and proposed pixel circuits as V_{DD} transitions from 7 to 4 V.

The currents exhibit disparity between the proposed circuit and the conventional one, primarily due to data voltage mismatch affecting the pixel current. The conventional circuit employs a data voltage of 7 V, whereas the proposed circuit utilizes 4 V, as shown in Figures 7 and 8. The decision to employ a lower data voltage in the proposed pixel circuit was influenced by the bootstrapping mechanism. Initially, the data voltage is stored at Node P and subsequently boosted upon inputting Scan n + 1. This bootstrapping process leads to a significant rise in pixel current when Scan n + 1 is applied, as depicted in Figure 7. This current jump effectively demonstrates the occurrence of bootstrapping at Node P. However, even with bootstrapping, the effort fell short in equalizing the pixel currents with those of the 2T1C configuration, leading to unequal currents between the proposed pixel and the conventional 2T1C pixel.

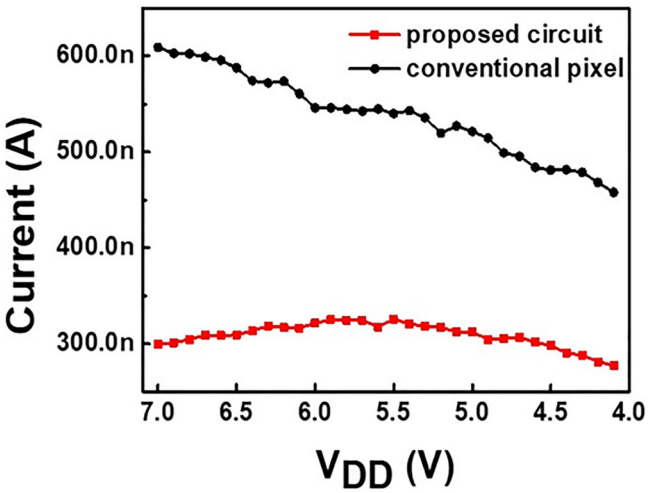


FIGURE 9 Comparison of the pixel current changes by V_{DD} between the proposed and conventional pixel circuits.

TABLE 3 Pixel currents by the changed V_{DD} of pixel circuits.

V_{DD}	Conventional pixel circuit	Proposed pixel circuit
7 V	608.9 nA	299.6 nA
4 V	457.9 nA	277.2 nA
Decrease	24.8%	7.5%

The currents for the conventional pixel circuit measured 608.9 nA at $V_{DD} = 7$ V and 457.9 nA at $V_{DD} = 4$ V. This represents a 24.8% decrease in current when transitioning from $V_{DD} = 7$ V to $V_{DD} = 4$ V. In contrast, the proposed pixel circuit exhibited currents of 299.6 nA at $V_{DD} = 7$ V and 277.2 nA at $V_{DD} = 4$ V, reflecting a more modest 7.5% reduction compared to $V_{DD} = 7$ V. Specifically, the currents for the proposed pixel circuit were 269.6 nA at $V_{DD} = 7$ V and 247.2 nA at $V_{DD} = 4$ V, representing a 7.5% decrease in response to the V_{DD} drop from 7 to 4 V. This reduction is notably smaller than the 24.8% observed for the conventional pixel circuit. However, in the conventional circuit, the drive TFT shifts to the triode regime due to the decrease in V_{DD}. Consequently, there is a reduction in currents as V_{DD} decreases, since the data voltage of 7 V surpasses V_{DD} as it changes from 7 to 4 V. Hence, in the conventional circuit, reducing V_{DD} is not permissible to maintain the saturation regime. On the contrary, in the proposed circuit, with a data voltage of 4 V, V_{DD} can be further reduced while still maintaining the saturation regime. Hence, the pixel currents in the proposed circuit remain relatively constant, with only a slight initial increase. This slight increase can be attributed to the heightened bootstrap to Node P, as outlined in Equation (2), where the reduction in V_{DD} leads to an increase in current. After that, the currents show a slight decrease as decreasing V_{DD}. This phenomenon can be attributed to the transition of the TFT to the triode regime, wherein the current decreases as the drain voltage decreases while remaining constant in the saturation region. Table 4 presents a comparison of the proposed IR drop compensation pixel circuits with other methods.

The ability to decrease both the data voltage and V_{DD} represents a significant advantage in terms of power consumption. Given that power consumption is proportional to the square of the voltage, the decreased voltage effectively reduces power consumption. Even though the proposed circuit lowers data voltages, it does not reduce OLED power consumption due to the boosting process at the node-P voltage. However, in the case of the data drive IC, using a lower voltage can lead to power savings. Additionally, the power consumption associated with charging and discharging the parasitic capacitances of the data lines can be reduced due to the lower data voltages. Consequently, the proposed pixel circuit offers lower power consumption compared to the conventional one.

A simulation was conducted utilizing the RPI LEVEL = 35 model, which was tailored to reflect the characteristics of the fabricated a-IGZO TFT and adjusted to account for the nonuniformity in terms of threshold voltage and mobility. Figure 10A,B provide a comparative

TABLE 4 Comparison of the proposed pixel circuit with other works.

Reference	Structure	V_{TH} compensation	IR drop compensation	OLED current error rate (ΔV_{DD})
[32]	6T2C LTPS	Y	Y	8.92% (−0.5 V)
[33]	5T1C LTPS	Y	Y	3.96% (−0.5 V)
[34]	5T2C IGZO	Y	Y	4% (±10%)
This work	4T2C a-IGZO	Y	Y	7.5% (−3 V)

Abbreviation: Amorphous indium-gallium-zinc-oxide (a-IGZO).

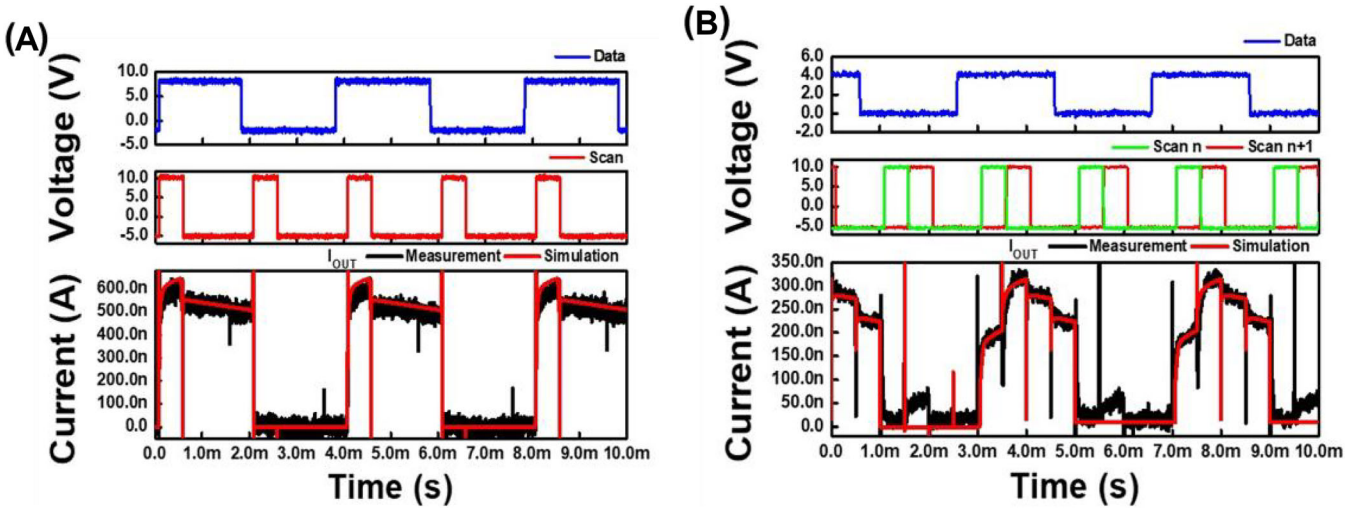


FIGURE 10 Comparison between the measurement and simulation results, (A) the conventional pixel circuit and (B) the proposed pixel circuit.

analysis of pixel circuits for each type through simulation and measurement.

Figure 10B illustrates the impact of stretching compensation during Scan n + 1, contrasted with Figure 10A, through both simulation and measurements. A scan pulse of 500 μs was employed, considering the observability of the measurement circuit.

Based on the simulation results, we evaluated the operational capability with shorter pulse widths. For practical applications, the pulse width must be sufficiently small. However, the fabricated TFT exhibits significantly low mobility due to the SU8 gate insulator and sub-optimal environmental conditions. The experiments in this paper exhibits a long pulse width due to the slow charging and discharging associated with low mobility of the oxide TFT. Typically, low mobility results in slower charging and discharging. However, since the primary compensation is achieved through capacitive coupling—an effect independent of the on-current—we expect the circuit to charge and discharge more rapidly with higher mobility TFTs. Therefore, our goal is to enhance mobility to further improve the response time. While we work on improving the TFT characteristics in the circuit, we have

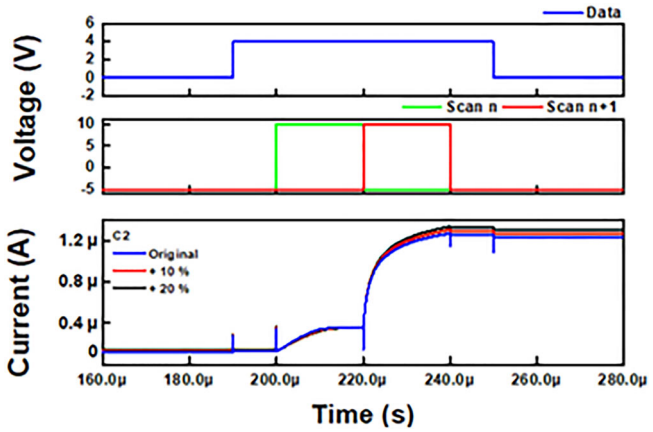


FIGURE 11 Simulation results for shorter pulse width with improved mobility.

simulated the performance with an increased mobility of 15 $cm^2/V{\cdot}s$, as shown in Figure 11.

Due to the low mobility of the TFT, the charging and discharging times are prolonged, making it impossible to operate with a short pulse. As a result, measurements were conducted using a longer pulse width. However,

with higher mobility, it becomes feasible to use a shorter pulse width as shown in Figure 11.

The efficacy of the stretching compensation was quantified using a circuit based on the 2T1C architecture in this paper. For its application in displays, it is essential to enhance the stretching compensation circuit by integrating a mechanism for compensating threshold voltage. The conventional compensation scheme designed to address the threshold voltage variation of T2 can be readily applied here. The suggested stretching compensation circuit easily integrates into standard internal compensation configurations, as illustrated in Figure 12A, commonly found in smartphones employing P-channel LTPS TFTs. Data input is denoted by the dotted arrow in Figure 12A, with the data voltage undergoing compensation during the charging of the storage capacitance. The compensation circuit illustrated in (B) is well-suited for our proposed circuit, especially in the case of N-channel oxide TFTs. In this configuration, threshold voltage compensation is facilitated during the discharge of the initially stored voltage, as highlighted by the dotted arrow. In larger displays, such as TVs utilizing oxide TFTs, external compensation is typically employed to manage threshold variation in the drive transistor. Incorporating a readout bus, readout switching TFT, and a readout scan effectively compensates for the threshold variation of the drive transistor T2 as well as stretching compensation, as shown in Figure 12C.

In the instance of T4, using a diode type was intended to reduce bus line number, yet, it introduces a voltage drop during the transmission of the scan voltage. This concern can be addressed by introducing an additional bus line, as shown in Figure 13.

The reference voltage is employed to charge Node Q instead of using a diode structure. This approach not only avoids threshold voltage issues but also allows for precise control over the compensation effect by adjusting the reference voltage, thereby stabilizing variations in Node Q voltage. To achieve this, the high voltage of Scan n + 1 must exceed Vref by at least the threshold voltage.

The effectiveness of the proposed pixel circuit was evaluated using an internal compensation circuit, demonstrating its suitability as a compensation circuit for the threshold voltage of the drive TFT as shown in Figure 14. The circuit simulation was conducted to show how changing the threshold voltages for all the TFTs in the circuit affects its performance.

The figure presents pixel current and current error rates for different Vth and increased capacitance of C2. The error rate for current variation due to Vth fluctuation was defined using Equation (4).

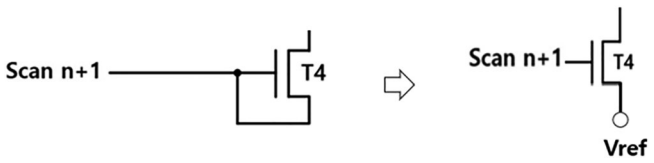


FIGURE 13 The diode scheme of T4 introduces threshold voltage-dependent variations, which can be resolved by supplementing additional voltage Vref for the drain voltage.

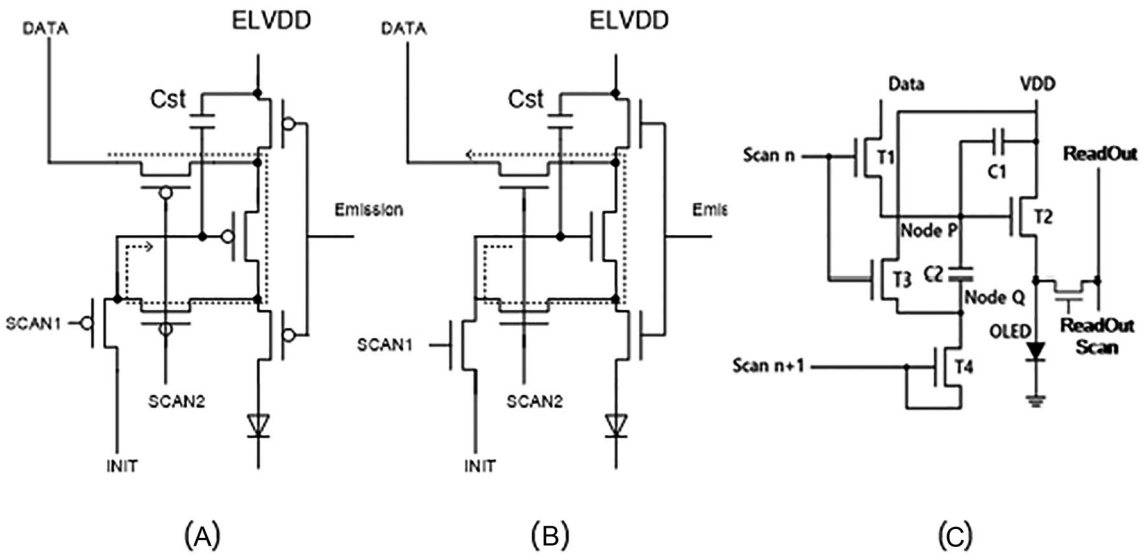


FIGURE 12 Typical compensation schemes for addressing threshold variation in the drive thin-film transistor (TFT), (A) conventional LTPS TFT compensation circuit, (B) internal compensation scheme with N-channel TFTs, (C) external compensation scheme that incorporates stretching compensation.

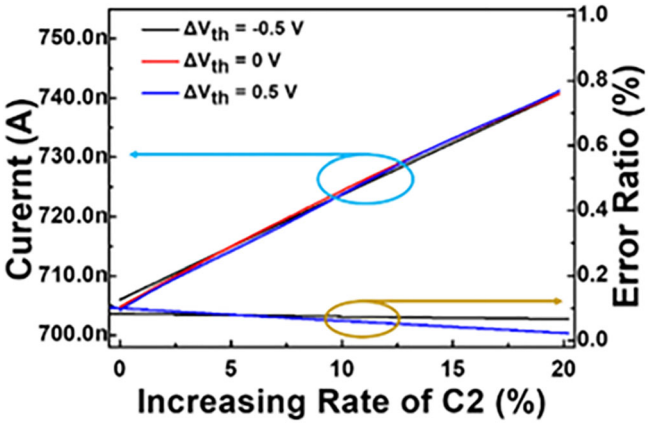


FIGURE 14 Pixel currents of the pixel circuit and the current error rate due to variations in Vth while increasing capacitance.

$$\frac{|I_{\Delta Vth=0} - I_{\Delta Vth\pm 0.5\,V}|}{I_{\Delta Vth=0}} \times 100(\%) \quad (4)$$

In the examined pixel circuit, the OLED current exhibited an increase with the rise in the capacitance of C2, irrespective of Vth variation. This increase, in accordance with Equation (3), effectively compensated for luminance imbalances caused by increased pixel spacing. Notably, the current error rate due to Vth variation remained below 0.1%, even with a 20% increase in the capacitance of C2.

The linearity between the pixel currents and the capacitances of C2 is important. While Figure 14 reveals a slight deviation from perfect linearity, the pixel current measurements provided in Table 1 indicate that doubling the capacitance of C2 led to a current increase ranging from 16.9% to 24.1%. Notably, this increase was less than a direct doubling of the capacitance. The difference highlights the necessity for further research to thoroughly investigate the linearity aspect. When addressing luminance compensation, it is crucial to investigate the correlation between luminance and pixel current. A comprehensive engineering analysis of the linearity between luminance and pixel current is indispensable and calls for additional rigorous research efforts.

5 | CONCLUSIONS

The pixel circuit was designed to address luminance variations resulting from area stretching in stretchable AMOLED displays. The proposed circuit effectively compensates luminance imbalances induced by the expanded area during stretching. The proposed pixel circuit comprises four a-IGZO TFTs, one storage capacitor, and one stretching-dependent capacitor. Fabrication of pixel circuits using a-IGZO was undertaken to validate the compensation mechanism of the proposed design. Three variations of pixel circuits, featuring sense capacitances of 0.10, 0.11, and 0.12 pF, were specifically manufactured to assess compensation for area stretching. The measured output currents for capacitances of 0.10, 0.11, and 0.12 pF were 378.1, 441.8, and 469.2 nA, respectively. The current exhibited an increase ranging from 16.9% to 24.1% with the rise in sense capacitor capacitance from 0% to 20%. The data and power voltages (V_{DD}) could be reduced compared to those in the conventional circuit. Consequently, the proposed pixel circuit offers lower power consumption compared to the conventional one. Both measurement and simulation results validate the compensation capability of the proposed pixel circuit for area expansion.

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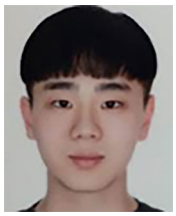

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