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ORIGINAL ARTICLE - ELECTRONICS, MAGNETICS AND PHOTONICS

Low Voltage a-IGZO Thin Film Transistor Using Tantalum Oxide by Thermal Oxidation

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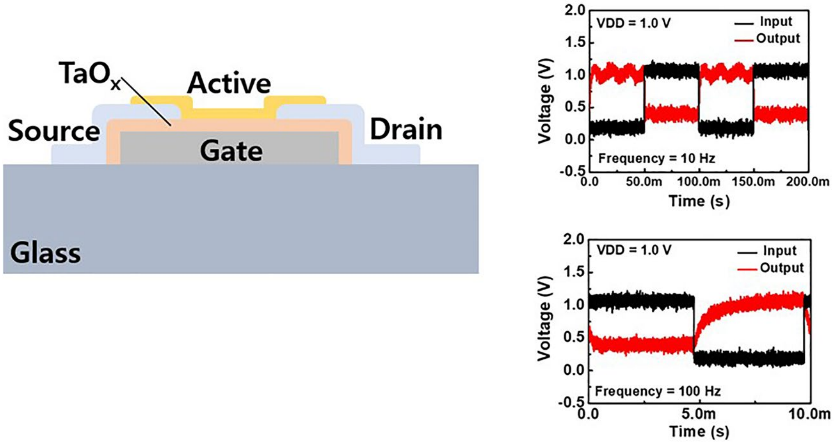
Abstract

Low voltage oxide thin-film transistors (TFTs) operating below 1.0 V were developed using a high dielectric constant tantalum oxide produced by thermal oxidation. Thermal oxidation was carried out at 400, 500 and 600 °C under an oxygen atmosphere. The tantalum oxide was evaluated by X-ray photoelectron spectroscopy (XPS). XPS confirmed the binding energy of Ta4f, indicating the binding state of tantalum oxide. The bottom gate oxide TFT with the gate insulator of tantalum oxide grown at 500 °C exhibited mobility of 26.7 cm^2/V s and a threshold voltage of 1.3 V. The transfer characteristics at the drain voltages below 1.0 V show its applicability to low voltage operation below 1 V. The bootstrapped inverter with developed oxide TFTs operated well at the 1.0 and 2.0 V operation voltages.

Graphical Abstract



Keywords Low voltage · a-IGZO TFT · Thermal oxidation · Tantalum oxide

1 Introduction

Thin-film transistors (TFTs) are used widely in the backplane of flat panel displays. In addition to hydrogenated amorphous silicon (a-Si:H) TFTs for active-matrix liquid crystal display (AMLCD), low-temperature polysilicon (LTPS) TFTs are being used for organic light-emitting diode (OLED) displays. Oxide TFTs are used for large-sized OLED displays, such as televisions, owing to the low-cost and straightforward

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process on large glass substrates compared to LTPS TFTs [1, 2]. An amorphous IGZO (indium–gallium–zinc–oxide) TFT is the most popular oxide TFT.

In addition to display applications, TFTs are being evaluated for various applications, such as sensors [3], radio frequency identification (RFID) [4], and flexible wearable devices [5]. A requirement for mobile applications is low power consumption. To achieve low power consumption, the operation voltage should be decreased because the power consumption is proportional to the square of the operation voltage. The operation voltage should be higher than the threshold voltage. Therefore, the threshold voltage of oxide TFTs should be decreased to achieve low power consumption [6].

The threshold voltage can be reduced by increasing the capacitance of the gate insulator, which is achieved by decreasing the thickness or increasing the dielectric constant of the gate insulator [6–8]. In the case of aluminum oxide, it is a representative high dielectric constant material and was used by being applied to a-IGZO TFT [9–11]. The decrease in thickness and increase in dielectric constant increase the induced charge in the channel caused by the increased gate capacitance. This, in turn, results in a decrease in the threshold voltage of the TFT and enables the low-voltage operation of the TFT. For high-level dielectric constant gate insulators, ionic liquids or ion gels were studied for low-voltage operation transistors, and they usually exhibit pool chemical stability [12, 13].

A one-volt IGZO TFT was reported using a thin (3 nm) gate insulator of anodized aluminum [14]. They formed a 2–3 nm aluminum oxide film by anodic oxidation in an electrolyte of 1 mM citric acid and obtained a low threshold voltage of 0.43 V with mobility of 5.6 $cm^2/V\cdot s$. One advantage of anodic oxidation is a low-temperature process suitable for flexible substrates. Many high dielectric materials have been studied [15–19], and half-volt operation IGZO TFTs with an ultrathin HfO_2 gate insulator were reported [20]. Hafnium oxide shows a dielectric constant that is 20–25 higher than the ~9 for aluminum oxide. They used atomic layer deposition to obtain 5 nm hafnium oxide for a gate insulator and accomplished a low threshold voltage of 0.3 V with an operating voltage of 0.5 V.

A tantalum oxide layer also has a large dielectric constant of 22 and has been applied as the gate insulator using various methods, such as sputtering, anodic oxidation, sol–gel, e-beam evaporation, thermal oxidation, and atomic layer deposition [21–25]. Threshold voltage reduction for organic TFTs was reported using anodized tantalum oxide as a gate insulator, and mobility of 0.36 $cm^2/V\cdot s$ was obtained on a plastic substrate [21]. A ZnO TFT with a sputtered Ta_2O_5 gate insulator was reported to have a mobility of 46.2 cm^2/V s [22]. They used a stacked gate insulator with the structure SiO_2 (5 nm)/Ta_2O_5 (50 nm)/SiO_2 (5 nm) by RF magnetron sputtering to solve the drawbacks of a high dielectric constant insulator, such as the leakage current and high concentration of charge trap. Martins et al. suggested Ta_2O_5/SiO_2 multi-component dielectrics for amorphous oxide TFTs to achieve both high dielectric constant and low defect density [23]. They produced the multi-component dielectric films by co-sputtering from Ta_2O_5 and SiO_2 targets. As the percentage of tantalum oxide increases, the permittivity of the multi-component dielectric was increased, and the field-effect mobility was decreased slightly due to the increased tantalum oxide. Chiu et al. used a 200 nm tantalum oxide layer evaporated by e-beam at room temperature as the gate insulator of ITZO TFT to achieve a low threshold voltage of 0.25 V with an operating voltage of 2 V [24]. Xu et al. reported a decrease in the threshold voltage of InAlZnO (IAZO) TFTs by changing the gate insulator from a thermally grown 100 nm SiO_2 to sputtered 70 nm Ta_2O_5. The threshold voltage for the Ta_2O_5 gate insulator was 1.24 V, whereas it was 4.07 V for the SiO_2 gate insulator [25].

Because tantalum oxide by anodic oxidation has a high dielectric constant and is a room-temperature process, it was used as the gate insulator of the thin-film transistors for low operation voltage and film substrates [21, 26]. Hafnium anodic oxidation was also used for the low voltage a-IGZO TFT [27]. On the other hand, thermal oxidation requires a high-temperature process but provides a denser oxide. Thermal growth usually shows superior quality to PVD or CVD and shows lower porosity [28]. Therefore, thermally grown Ta_2O_5 is preferable to deposited Ta_2O_5 in terms of its electrical property. Even tantalum oxidation was investigated [29–32], but its application to TFTs was not reported. Thermal oxidation of Ta was studied in the temperature range from 300 to 700 °C [29], which showed that the growth rate of the oxide is logarithmic at 300 °C and parabolic at 500 °C. They used Auger depth profiling to reveal that the metallic film oxidizes to first form low valence oxides of Ta that progressively convert to tantalum pentoxide with increasing temperature and time. With the sputtered Ta film, thermal oxidation was done at the oxidation temperatures from 673 to 873 K [31], and reported the dielectric constant as high as 25–32. The Gibbs free energy of Ta_2O_5 is − 1911.2 kJ/mol which is much lower than − 533.0, −888.8 and − 1582.3 kJ/mol for MoO_2, TiO_2 and Al_2O_3, respectively. And it is much lower also than − 856.4 kJ/mol of SiO_2. Therefore, the thicker oxide can be easily obtained with Ta than other metals such as Mo, Ti, and Al under the same oxidation condition. A 22 nm and 210 nm tantalum oxide layers were obtained after 100 min oxidation at 300 and 500 °C, respectively [29].

Building upon previous research into the thermal oxidation of Ta, we have developed the first IGZO TFT that incorporates thermal tantalum oxide, taking advantage of its high dielectric constant. Thermal oxidation, unlike the deposition of various insulators such as silicon dioxide, silicon nitride, and aluminum oxide, does not require the use of vacuum equipment and results in a dense oxide that is useful for the gate insulator. Moreover, thermal oxidation can produce a uniform thickness of thin tantalum oxide, which is difficult to achieve through deposition methods. The high dielectric constant and uniform thin oxide layer make it easier to achieve low voltage operation of the TFT. In this study, we developed low-voltage a-IGZO TFTs by employing thermal oxidized tantalum oxide as the gate insulator and In-rich IGZO for high performance [33–36].

2 Experiments

For XPS analysis, the thermally grown tantalum oxide layer was produced by depositing an 80 nm thick tantalum layer on a *p*-type silicon wafer by DC magnetron sputtering, followed by oxidation for 20 min in an oxygen atmosphere at three temperatures (400, 500 and 600 °C). Thermally grown tantalum oxide was analyzed by XPS.

For C–V analysis, the Ta layer was fully oxidized after depositing on the *p*-type silicon wafer. After depositing a 1.5 mm diameter Al electrode using a shadow mask, the C–V characteristics were measured using an LCR meter.

The process of a-IGZO bottom gate TFT using the developed thermal growth tantalum oxide is as follows. A 300 nm thick tantalum gate layer was deposited by DC magnetron sputtering and patterned as the gate electrode by dry etching using fluorine gas. Subsequently, annealing was performed at 500 °C in an oxygen atmosphere to generate a tantalum oxide gate insulator layer. After oxidizing tantalum, Indium tin oxide (ITO) was used as the source and drain electrodes and was deposited by RF magnetron sputtering. The working gas pressure was 5.5×10^{-3} Torr, and the Ar and O_2 flow rates were 19 and 1 sccm, respectively. And the ITO S/D layer was post-annealed for 1 h in ambient air at 200 °C. The wet etchant was aqua regia. A 30 nm a-IGZO layer was deposited at 250 °C by RF magnetron sputtering using an In:Ga:Zn = 2:1:2 (mole ratio) target. The working gas pressure was 5.5×10^{-3} Torr, and the Ar and O_2 flow rates were 22.5 and 7.5 sccm, respectively. The active IGZO layer was defined by photolithography during the IGZO deposition. The IGZO layer was post-annealed in the O_2 ambient at 250 °C for 1 h.

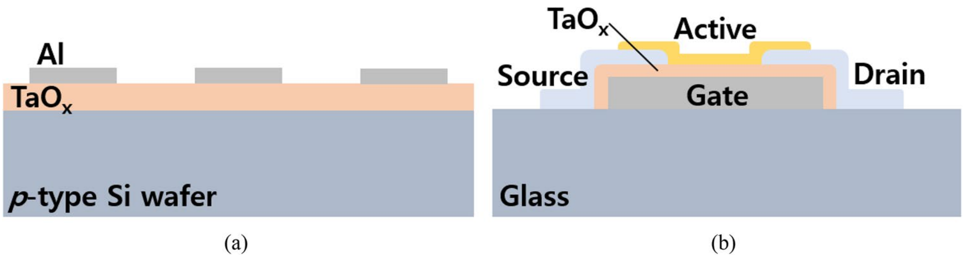
3 Results and Discussions

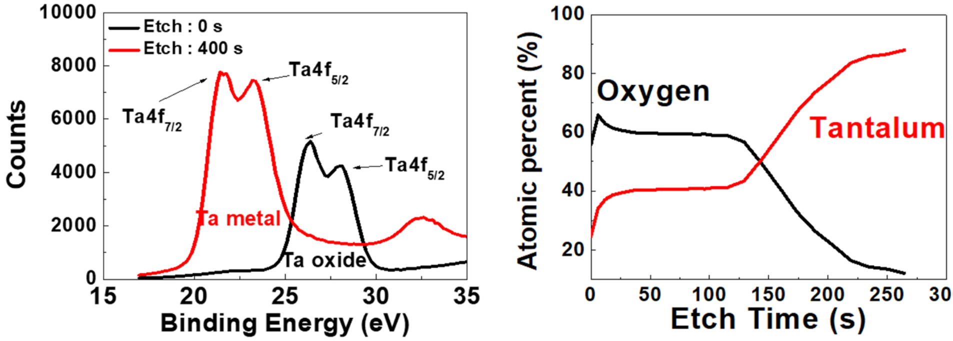
A metal–oxide–semiconductor (MOS) structure and a bottom gate structure IGZO TFT were fabricated on a silicon and a glass substrate, respectively as shown in Fig. 1a and b. In the case of the MOS structure, thermal oxidation was performed after depositing tantalum on *p*-type silicon by sputtering. The tantalum was fully oxidized to measure the C–V characteristics. The upper electrode was then deposited as a dot with a diameter of 1.5 mm using a shadow mask during metal deposition by sputtering.

In this study, tantalum oxide was applied to the gate insulator which has a decisive effect on device performance in terms of threshold voltage, subthreshold slope, bias stability, and so on. Before applying the tantalum oxide to the device, we evaluated the thermal oxidized tantalum oxide. To evaluate a tantalum oxide, a 300 nm thick Ta film on a silicon wafer was annealed in a furnace at 400, 500 and 600 °C for 20 min under an oxygen atmosphere to form tantalum oxide. After the oxidation of tantalum, XPS (X-ray photoelectron spectroscopy) was carried out while etching the film to obtain a depth profile as shown in Fig. 2a and b. Figure 2a presents the XPS spectrum of the tantalum oxide oxidized at 500 °C for 20 min under an oxygen atmosphere. At the surface, the binding energy of $Ta4f_{7/2}$ and $Ta4f_{5/2}$ were approximately 26.4 and 28.6 eV, respectively, which correspond to tantalum oxide. After an etch time of 400 s, the peaks shifted to ~ 21.5 eV and ~ 23.3 eV, which are typical peaks for tantalum metal. Figure 2b presents the atomic percentage according to the etch time. As the etch time increased, the oxygen concentration decreased, and Ta increased, which shows the oxidized tantalum on the surface of the Ta film.

Figure 3a presents the XPS spectrum of O1*s* in tantalum oxide shown in Fig. 2b. The O1*s* peak was deconvoluted from three Gaussian peaks centered at O_I (530.1 eV), O_{II} (530.6 eV), and O_{III} (531.5 eV). The O_I, O_{II}, and O_{III} peaks correspond to the tantalum–oxygen bond, oxygen

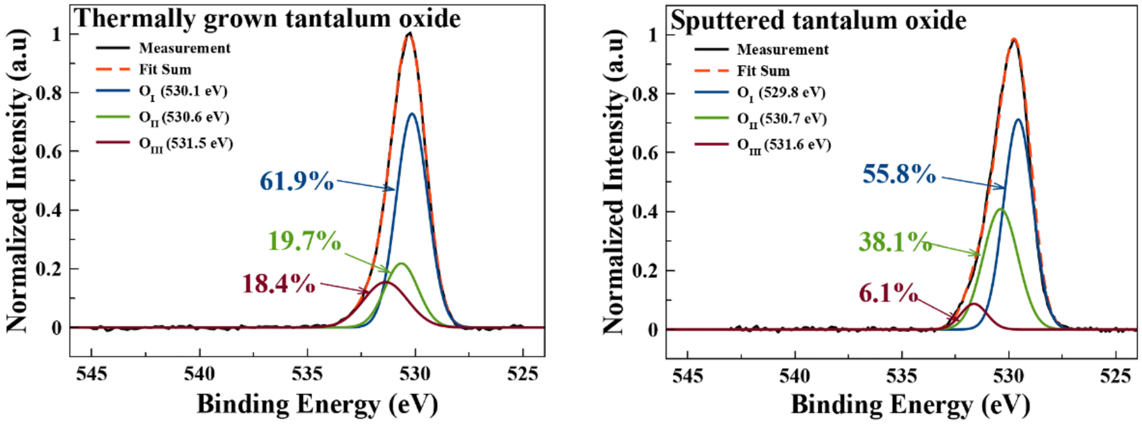
Fig. 1 The cross-sectional structure of the fabricated MOS structure (**a**), and the low voltage bottom gate a-IGZO TFT





(a) (b)

Fig. 2 XPS results for thermally grown tantalum oxide, **a** shows the binding energy, and **b** the depth profile for the atomic compositions of oxygen and tantalum



(a) (b)

Fig. 3 XPS spectrum for O1*s* of tantalum oxide, **a** O1*s* peak of tantalum oxide thermally grown at 500 °C and **b** O1*s* peak of tantalum oxide by sputtering

vacancy-related one, and surface-oxygen related to adsorbed H_2O, respectively. For comparison with sputtered tantalum oxide, XPS data were obtained for the sputtered tantalum oxide as shown in Fig. 3b. Tantalum oxide by thermal oxidation showed larger, and sharper O_I peaks and smaller O_{II} and O_{III} peaks than tantalum oxide by sputtering, which denotes fewer defects in the thermal tantalum oxide than the sputtered one, making it preferable for a gate insulator [32].

We annealed at different temperatures under a fixed oxidation time condition to observe the thickness of tantalum oxide. Figure 4 shows the oxide thickness of thermally grown tantalum oxide. Our observations indicate a clear correlation between the thickness of the oxide film and the temperature, as the thickness increased with the rise in temperature. It should be noted that the thickness of tantalum oxide, formed via the thermal oxidation of tantalum, is significantly influenced by both the duration and temperature of the process. The thickness of the oxide layer formed through thermal oxidation is highly dependent on the oxidation time, as well as other factors such as temperature, gas flow rate, and pressure.

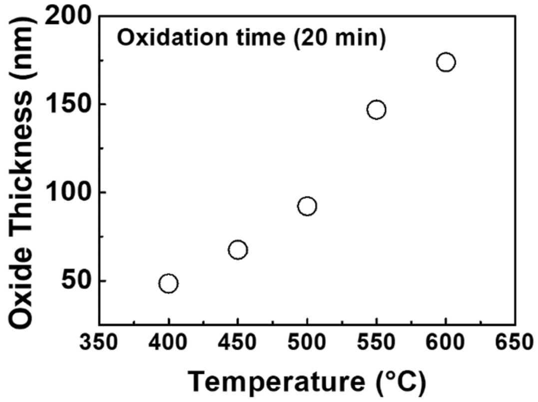


Fig. 4 The thickness of tantalum oxide grown through thermal oxidation

In general, the thickness of the oxide layer increases with increasing oxidation time, as the oxygen has more time to diffuse into the tantalum surface and react with the metal. However, the rate of oxide growth may slow down as the oxide layer gets thicker due to a decrease in the oxygen diffusion rate. The reaction between oxygen and tantalum also affects the oxidation rate, which makes the oxidation rate more complex. According to Park et al., the growth rate of the oxide layer on tantalum has been found to follow a logarithmic trend at 300 °C and a parabolic trend at 500 °C [29]. These growth rates and the transition from one growth type to another strongly correlate with changes in both the surface and film morphology, as well as the reactivity and diffusivity of the matrix with temperature. These factors are known to have a significant impact on the oxide layer growth kinetics, and a thorough understanding of the growth mechanisms is essential for optimizing the thermal oxidation process of tantalum.

Tantalum oxide by thermal oxidation showed larger, and sharper O_I peaks and smaller O_{II} and O_{III} peaks than tantalum oxide by sputtering, which denotes fewer defects in the thermal tantalum oxide than the sputtered one, making it preferable for a gate insulator [32]. Oxygen diffuses through tantalum from the surface during heat treatment in an oxygen atmosphere. The diffused interstitial oxygen reacts to form a low-valance oxide at first. It is known that tantalum reacts fast to form an intermediate Ta_2O with great compressive stress due to the volume expansion and then the intermediate tantalum oxide transforms to the Ta_2O_5 slowly and releases the stress due to the amorphous properties of Ta_2O_5. Therefore, the low valance oxide Ta_2O and Ta_2O_5 coexist in the layer. The ratio between them depends on depth, oxidation temperature, and time. The depth profiles of XPS spectra were obtained by gradual etching of the sample during measurement. The spectra were fitted using Gaussian peaks associated with Ta_2O_5 and Ta_2O. The obtained depth profiles of Ta_2O_5 and Ta_2O are shown in Fig. 5a and b. As the etch level was increased, the peak for Ta_2O_5 decreased, and the peak for Ta_2O increased. Ta_2O_5 ratio to Ta_2O decreases as depth increases due to the oxygen diffusing from the surface. Since the oxidation temperature affects the diffusion and oxidation, the Ta_2O_5 ratio increases with increasing temperatures and decreases for Ta_2O. Tantalum is oxidized to stoichiometric tantalum oxide at the surface by the sufficient oxygen supply. On the other hand, the Ta_2O peak increases as far away from the surface due to the lack of oxygen. For the stoichiometric bond, an increase in annealing temperature and time is required.

Figure 6 shows the I–V characteristics of tantalum oxide. The red, blue, and green lines are for tantalum oxide grown at 400, 500 and 600 °C, respectively. Two points were measured and showed resemble results. At the dielectric breakdown, an abrupt current increase was observed. The abrupt current increase occurred at ~20, ~42 and ~140 V, respectively. The increased thickness and more stoichiometric structure with increasing temperature can explain the increased breakdown voltages. In terms of leakage current, we can define the breakdown voltage at which the current density reaches 1 μA/cm^2. By this definition, the breakdown voltages are ~8, ~15 and ~50 V, respectively. In the case of the tantalum oxide layer grown at 400 °C, the leakage breakdown voltage is too low to be used in devices, while the leakage breakdown voltage of ~15 V for the layer grown at 500 °C is rather useful for electric devices, especially for the low voltage operation under 2 V.

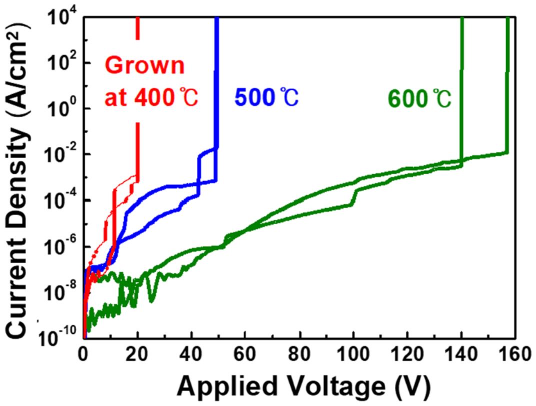
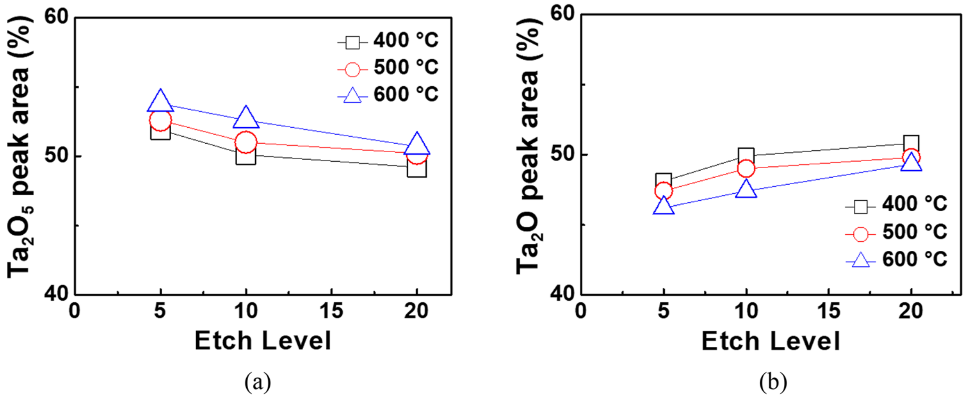


Fig. 6 I–V characteristics of tantalum oxide layers grown thermally at 400, 500 and 600 °C

Fig. 5 Ta_2O_5 and Ta_2O ratios are shown in these figures, **a** shows Ta_2O_5 peak area and **b** shows the Ta_2O peak area for several oxidation temperatures



(a)

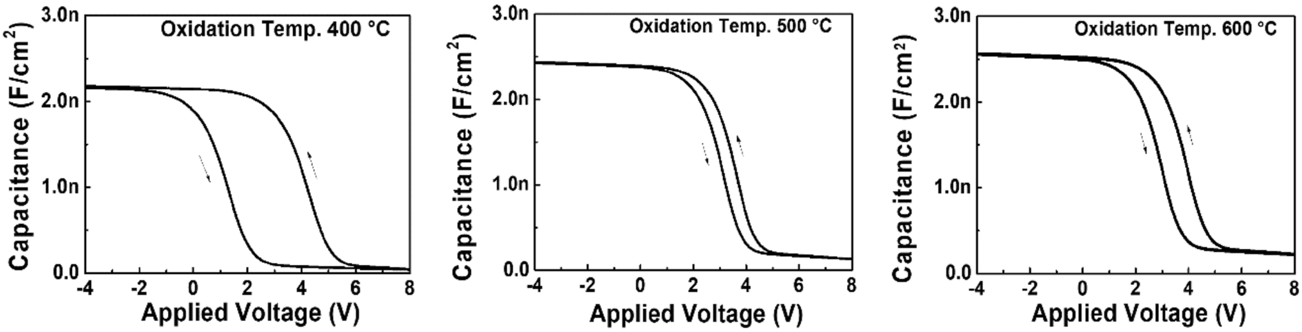
(b)

Figure 7 shows the C–V characteristics of thermally grown tantalum oxide on the *p*-type silicon wafer with a circular metal top electrode as shown in Fig. 1a. Figure 7a–c are for tantalum oxide grown at 400, 500, and 600 °C, respectively. The flat band capacitances were 2.15 nF, 2.43 nF and 2.56 nF, respectively. The dielectric constants were 15.8, 17.6 and 18.7, respectively. The increasing capacitance with increasing oxidation temperature can be explained by increased dielectric constant. The oxidation of tantalum occurred by oxygen diffusion into the Ta as interstitial and then Ta and oxygen form tantalum oxide as an intermediate tetragonal Ta_2O crystal with great compressive stress due to the volume expansion. The intermediate tantalum oxide transforms to the amorphous phase of Ta_2O_5 rather slowly compared to the initial formation of intermediate tantalum oxide. During the formation of the Ta_2O_5, the stress is released due to the amorphous properties of Ta_2O_5. The voltage sweep was − 4 V to + 8 V and the frequency used for measurement was 100 kHz in the C–V measurements. The sweep voltage initially increased and then decreased to observe the hysteresis. The shifted voltages for the tantalum oxide layers grown at 400, 500 and 600 °C were 2.95, 0.35 and 0.8 V, respectively. As the oxidation temperature increased, tantalum oxide became more stoichiometric and less defective, which explains the reduced hysteresis for higher oxidation temperatures. For the sample processed at 600 °C, a slight increase in hysteresis was observed and attributed to some other effects such as thermal stress as reported by Chandrasekharan et al. [26]. They observed the small crack with increased roughness of the surface morphology during thermal oxidation at 700 °C. Even if the oxidation temperature is 600 °C which is lower than 700 °C, we can suspect increased defects during the oxidation. However, it needs further investigation which will be future research work. Since 500 °C oxidation gives less hysteresis and has an appropriate breakdown voltage for the low operation voltages below 2 V, it was adopted for the low-voltage oxide TFTs.

Figure 8a shows the transfer characteristics of the bottom gate IGZO TFT with a gate insulator using tantalum oxide grown at 500 °C for 20 min in an oxygen atmosphere. Equation (1) was used to derive the mobility and threshold voltage from the saturation current region:

$$I_{DS} = \frac{1}{2}\frac{W}{L}\mu_{FE}C_i(V_{GS} - V_{TH})^2 \tag{1}$$

Here, W and L represent the width and length of the TFT, respectively, while C_i is the capacitance per unit area of the tantalum oxide. V_{TH} and V_{GS} denote the threshold voltage and gate voltage relative to the source.



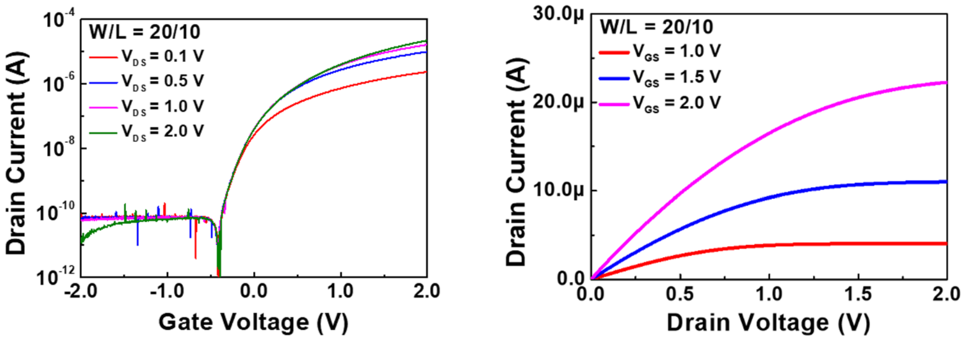
(a)

(b)

(c)

Fig. 7 C–V characteristics of the tantalum oxide layers grown at 400 °C (**a**), 500 °C (**b**) and 600 °C (**c**)

Fig. 8 **a** Transfer characteristics, and **b** output characteristics of the fabricated bottom gate IGZO TFTs with a gate insulator of tantalum oxide thermally grown at 500 °C for 20 min



(a)

(b)

The mobility extracted from the saturation region was 26.7 $cm^2/V \cdot s$ and the threshold voltage, subthreshold swing, and on–off ratio were 1.3 V, 0.24 V/dec, and 1.0×10^6, respectively. It shows the low voltage characteristics applicable to the operation voltages below 1–2 V. The output characteristics are shown in Fig. 8b. The inverter was designed for low-voltage operation and verified after fabrication.

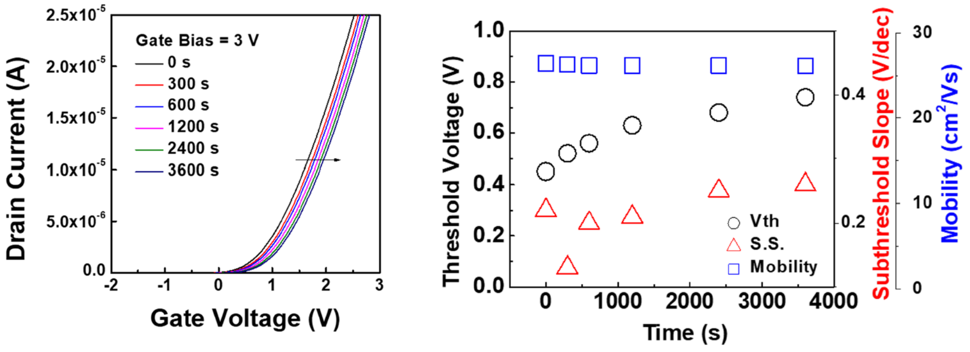
The positive bias stress (PBS) results are shown in Fig. 9a and b. The bias stress voltage was 3 V, and both the source and drain were grounded during bias stress. As the bias stress time increases, the curves shifted to the right as a threshold voltage increases due to the positive gate bias stress. The threshold voltage increase was 0.22 V after 3600 s. The mobilities changed from to 26.4–26.1 $cm^2/V \cdot s$ and the sub-threshold slope (S.S.) from 0.22 to 0.26 V/dec.

Figure 10a shows the bootstrapped inverter circuit with *n*-channel oxide TFTs. The W/L of the T1 and T2 transistors were 100/10 µm and 1000/10 µm, respectively. The W/L of the drive transistor T3 was 2000/10 µm. The bootstrap capacitor C1 had a capacitance of 0.6 pF. Figure 10b shows an optical microscopic image of the fabricated bootstrapped inverter.

Figure 11 presents the AC characteristics of the fabricated inverter shown in Fig. 10. A square wave was used, varying the frequencies from 10 Hz to 1 kHz. The high voltages of the input square waves were 1.0 and 2.0 V. Figure 9a–c are the AC characteristics for 1.0 V, and d–f are for 2.0 V. The power voltage VDDs were the same as the input high voltages. The successful inverter AC operations were observed, and the rise and fall times were shortened for a higher operating voltage of 2 V.

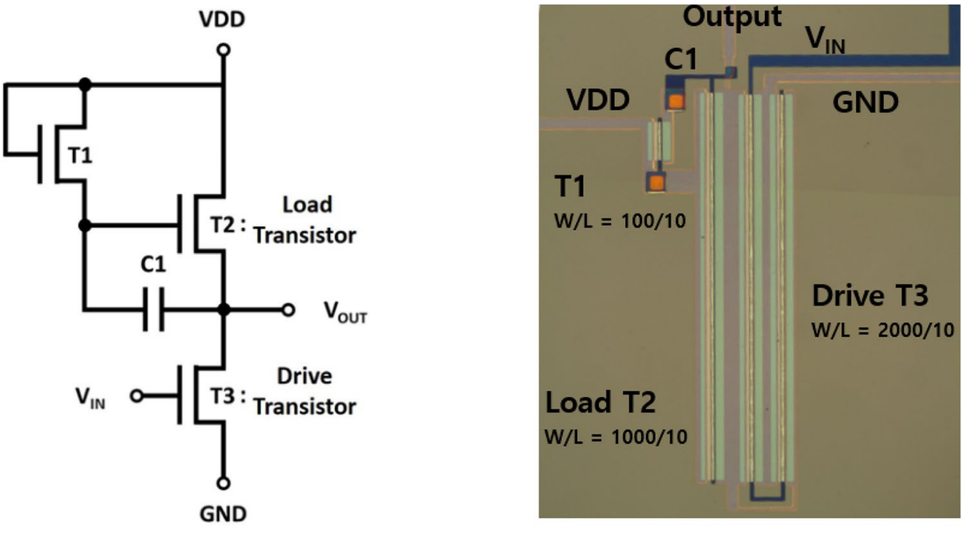
Figure 11a–c are for 1.0 V operation and their operating frequencies are 10, 100, and 1000 Hz, respectively. The rise and fall times are rather long and further research is needed to improve the rise and fall times, that is, the mobility should be improved and will be a future research activity. Figure 11d–f are for 2.0 V operation and operating

Fig. 9 Gate bias stabilities of the bottom gate IGZO TFTs with a gate insulator of tantalum oxide thermally grown at 500 °C, **a** transfer characteristics with a gate bias stress voltage of 3 V, **b** parameter changes by positive gate bias stress



(a) (b)

Fig. 10 The bootstrapped inverter circuit by *n*-channel IGZO TFTs (**a**), and fabricated bootstrapped inverter with a thermal tantalum oxide gate insulator (**b**)



(a) (b)

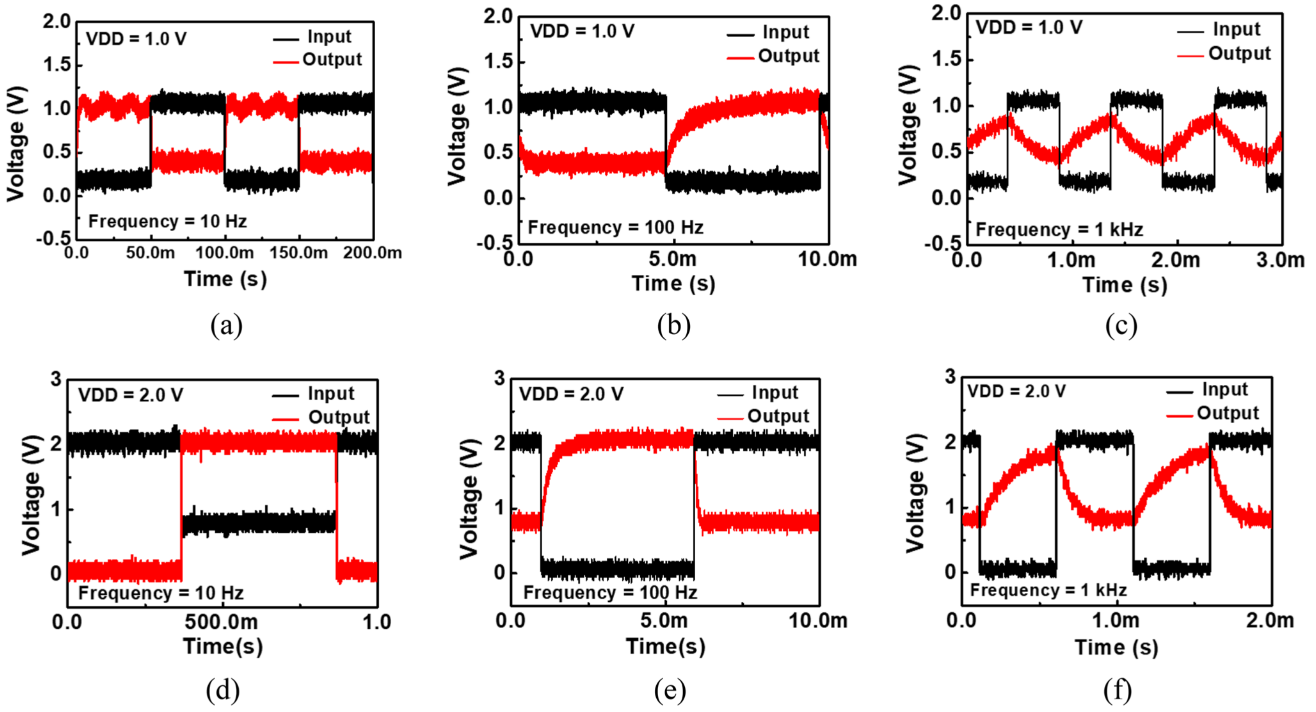


Fig. 11 AC characteristics of the developed low voltage inverter circuits, **a**, **b** and **c** are for 1.0 V operation and **d**, **e** and **f** are for 2.0 V operation

frequencies are 10, 100, and 1000 Hz. The rise and fall times are improved compared to the 1.0 V operation. In terms of output high voltages, the voltage drop was not observed due to the bootstrapping in the gate voltage of the drive TFT. In a conventional inverter circuit voltage drop is usually observed due to the threshold voltage loss in the load TFT. The gate voltage of the drive TFT is bootstrapped-up during the output high, which enables the full upswing of the output voltage without voltage loss. However, the offset was not improved, and an offset voltage of about 0.8 V was observed. The offset voltage can be improved by increasing the width of the drive TFT since the output voltage low is determined by the ratio of on-resistance of the drive TFT to that of load TFT.

4 Summary

A low voltage-operation bottom gate a-IGZO TFT was developed using thermally grown tantalum oxide as a gate insulator. Tantalum oxide was investigated for oxidation temperatures of 400 ℃, 500 ℃ and 600 ℃. XPS revealed a change in the composition of Ta_2O_5 to Ta_2O as it is far from the surface, which affects the electrical properties of tantalum oxide, such as the dielectric constant and capacitance of the insulator. The surface of the tantalum oxide layer revealed the Ta_2O_5 by the sufficient supply of oxygen; the oxygen content decreased, and Ta_2O increased, moving further from the surface.

The O1*s* peak of thermally grown tantalum oxide was sharper than sputter-deposited tantalum oxide, and the thermal tantalum oxide was applied to the bottom gate IGZO TFT. The mobility and threshold voltages of the TFT with the tantalum oxide gate insulator grown at 500 ℃ were 26.7 cm^2/V·s and 1.3 V, respectively. Subthreshold swing and on–off ratio were 0.24 V/dec, and 1.0×10^6, respectively. It shows the low voltage characteristics applicable to the operation voltages below 1 V.

The bootstrapped inverter circuits using the developed oxide TFTs were designed and fabricated. The fabricated bootstrapped inverter was verified with the operation voltages of 1.0 V and 2.0 V. At both the operation voltages, it operated well up to 100 Hz. To achieve higher operation frequencies, further research is necessary to increase the mobility for the gate insulator of thermally grown tantalum oxide.

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Declarations

Conflict of interest There are no conflicts to declare.

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