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Improving the electrical stability of a-IGZO TFT through gate surround structures

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This paper delves into a structural modification of dual-gate oxide thin film transistor (TFT). Diverging from the conventional dual-gate TFT structure, the authors' approach connects the bottom and top gate electrodes, effectively enveloping all four sides of the a-IGZO channel. This shielding configuration ensures stable operation, even under light illumination. Moreover, capitalizing on the stability under light conditions, the authors observed a remarkable threefold improvement in the mobility of the fabricated TFT with this proposed structure, resulting in a substantial 156% increase in current. Furthermore, in the negative bias illumination stress test, the proposed TFT exhibited minimal fluctuations when compared to its single-gate counterpart, further underscoring its exceptional and robust performance.

Introduction: Amorphous indium-gallium-zinc-oxide (a-IGZO) thin film transistor (TFT) offers a significant advantage over a-Si:H TFT in terms of higher mobility, while also surpassing LTPS (Low-Temperature Polysilicon) TFT in terms of larger area processing and lower cost [1]. The a-IGZO TFTs exhibit remarkable characteristics, including low power consumption and minimal leakage current, making them exceptionally well suited for a wide range of electronic devices, including sensors and wearable devices [2, 3]. Despite its advantages, a-IGZO technology still faces reliability challenges, particularly concerning illumination stress. To overcome the reliability issues associated with a-IGZO technology, researchers are diligently exploring multiple experimental avenues. These efforts encompass a broad spectrum of changes, with a focus on optimizing the materials used, introducing supplementary processes, and implementing structural enhancements [4–6].

In the top gate, dual gate (DG), gate surround (GS), and gate-all-around (GAA) configurations, the gate electrode is positioned on the top of the a-IGZO layer, acting as a light-blocking layer. This crucial feature shields the semiconductor material from external light, safeguarding its stability and performance under diverse lighting environments. By applying voltages simultaneously to the upper and lower gate electrodes, DG IGZO TFTs achieve a low turn-on voltage (V_{ON}) and enhance current flow. The formation of two channels through this dual-gate operation optimizes the electron transport within the device, resulting in increased efficiency and improved electrical characteristics.

In our research, the primary objective was to tackle the reliability issues associated with a-IGZO TFTs concerning light sensitivity. To achieve this, we pursued an innovative approach, incorporating a structure like the widely adopted GAA configuration used in Si-based TFTs, into oxide TFTs. This novel configuration not only led to improved mobility but also served the crucial role of acting as a light shield (LS).

Experiment: In our research, we achieved the successful fabrication of a-IGZO TFTs using a versatile 3-type structure. This structure comprises single-channel a-IGZO TFTs with both bottom-gate and bottom-contact (BGBC) and top-gate and bottom-contact (TGBC) configurations, as well as gate surround a-IGZO TFTs. Each of these structures offers distinct advantages and serves as a valuable foundation for exploring diverse applications and optimizing TFT performance. A bottom gate electrode, 200-nm-thick, was deposited using DC magnetron sputtering with Tantalum (Ta) as the material. An 80-nm-thick Al_2O_3 bottom gate insulator layer was deposited using atomic layer deposition (ALD) at a process temperature of 150°C. For source and drain electrodes, a 200-nm-thick indium tin oxide (ITO) layer was deposited by radio frequency (RF) magnetron sputtering using ITO target. An a-IGZO active layer 30-nm-thick was deposited by RF magnetron sputtering using a-IGZO (2:1:2 at %) target. The a-IGZO layer underwent post-annealing

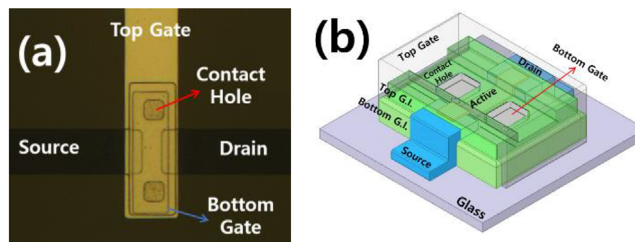

Fig. 1 *Structure of gate surround a-IGZO TFTs. (a) Microscopic optical image of a GS a-IGZO TFTs, (b) bird's eye view. a-IGZO, amorphous indium-gallium-zinc-oxide; GS, gate surround.*

Table 1. Parameters extracted for single and gate surround a-IGZO TFTs.

	μ_{FE} (cm^2/ V·s)	S.S. (V/dec)	V_{TH}-turn on (V)	I_{ON}/I_{OFF} ratio	ΔV (mV)
GS	32.3	0.39	3.94	7.9×10^6	0.1
BG	11.1	0.67	2.62	1.1×10^6	110
TG	11.2	0.52	3.51	2.8×10^6	30

a-IGZO, amorphous indium-gallium-zinc-oxide; BG, bottom gate; GS, gate surround; TG, top gate.

in O_2 environment at 250°C for 1 h. An 80-nm-thick layer of Al_2O_3 was deposited using ALD. Following this deposition, a contact hole was meticulously formed to establish the connection between both the bottom and top gate electrodes. For the fabrication of these contact holes, we utilized wet etching with phosphoric acid, ensuring that they extended down to the bottom gate metal. These holes were intentionally designed to maintain separation from the a-IGZO active layer. A 200-nm-thick Ta top gate electrode layer was deposited by DC magnetron sputtering. Figure 1a shows a microscopic optical image of the fabricated GS a-IGZO TFTs. Figure 1b displays the cross-sectional view. The proposed GS a-IGZO TFTs, much like the GAA configuration, possess inherent light-blocking properties thanks to their distinctive structure. The stability of the proposed GS a-IGZO TFTs was evaluated through negative bias illumination stress (NBIS) tests.

Measurement: These tests were conducted to validate the effectiveness of the GS structure in providing comprehensive protection to the device from external light on all four sides. NBIS testing was performed under a negative bias stress condition with simultaneous illumination of 1200 lux from a white LED source. All measurements were conducted at room temperature in a dark box.

Results and discussion: The GS structure has demonstrated superior performance when compared to the single bottom gate (SBG) or single top gate (STG) structures, as clearly depicted in Figures 2a and 2b, which represent the transfer characteristics and output characteristics, respectively. The GS TFT has approximately three times higher mobility and sharper subthreshold swing (S.S.) than the single gate (SG) TFTs. In Table 1, we present the extracted parameters for each TFT, providing a detailed summary of their specific attributes and performance metrics. The tabulated data serves as a valuable reference for comprehending the unique characteristics and behaviour of each transistor. Notably, GS structures generally exhibit an increase in mobility compared to SG structures, as the GS structure forms double channels instead of a single channel, leading to enhanced mobility [7, 8]. The GS TFT exhibits a noteworthy increase in mobility, showcasing a remarkable 156% rise in current at a driving voltage of 5 V, as clearly depicted inFigure 2a.

An additional significant advantage of the GS structure surfaced during NBIS measurements. The GS TFT, owing to the interconnection between the top gate and bottom gate, exhibits a light shielding effect. Notably, the V_{TH} shift observed in NBIS is primarily influenced by interface trap charges or internal defects within the a-IGZO material [9, 10]. Figure 3 depicts the NBIS results of (a) SBG TFT, (b) STG TFT, and (c) GS TFT. A stress voltage of −5 V was applied during the testing, and

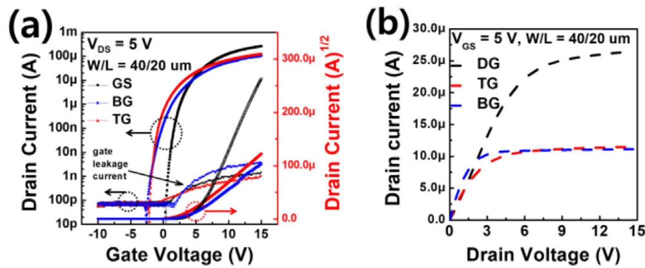

Fig. 2 *Comparison of electrical characteristics of the single and GS a-IGZO TFTs. (a) Transfer characteristics and (b) output characteristics. a-IGZO, amorphous indium-gallium-zinc-oxide; GS, gate surround.*

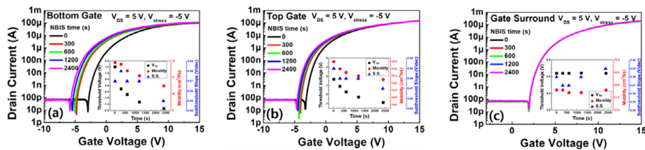

Fig. 3 *Negative-bias illumination stress of the a-IGZO TFTs. (a) SBG TFT, (b) STG TFT, and (c) GS TFT, a stress voltage of* -5 *V was applied. All TFTs are with channel width* $= 40$ μ*m and length* $= 20$ μ*m. a-IGZO, amorphous indium-gallium-zinc-oxide; GS, gate surround; SBG, single bottom gate; STG, single top gate.*

for the SG TFT, V_{TH} shifted by 4.65 V, along with a decrease in mobility to approximately 1.5 $cm^2/V{\cdot}s$.

When compared to the SG TFT, the GS TFT displayed exceptional stability, with an almost negligible V_{TH} shift approaching 0 V. The minimal variation observed in the proposed GS TFT can be attributed to its distinction from conventional GS structures. The unique feature of the proposed GS a-IGZO TFT lies in its ability to shield the a-IGZO active layer from light on all four sides achieved through lateral contact between the bottom and top gates. The light shielding effect played a crucial role in mitigating the impact of illumination on the device's performance, consequently enhancing the overall reliability and functionality of the TFTs. Additionally, the presence of interface trap charges on the back channel could also be a contributing factor. However, in the proposed GS structure, the connection between the bottom and top gate electrodes results in the formation of identical channels on both sides of the a-IGZO, ensuring a uniform distribution of trap charges. Consequently, the GS TFT exhibits enhanced stability and reliability compared to SG structures, such as SBG and STG TFTs [4, 11, 12].

Conclusion: To summarize, our research focuses on investigating the structural modification of a-IGZO TFTs through the incorporation of a GS structure. Our primary objective was to improve the devices' electrical characteristics and stability. Notably, the application of a GS structure, especially in the form of a GAA configuration, has not been extensively studied, rendering it an interesting and promising avenue for further exploration. By examining the potential advantages offered by this novel approach, we contribute valuable insights to the field and open new possibilities for advancements in a-IGZO TFT technology. The findings of our study reveal a significant three-fold enhancement in mobility for the GS a-IGZO TFTs, presenting a compelling advantage over conventional TFTs. Furthermore, the devices exhibited improved stability during NBIS testing, a crucial indicator of their robustness. These noteworthy improvements can be directly linked to the effective protection of the active layer. By thoughtfully placing gates on all four sides of the a-IGZO channel, the GS structure ensures comprehensive shielding of the semiconductor material from external influences, leading to superior device performance and long-term reliability. This innovative approach holds great promise in advancing a-IGZO TFT technology and opens up exciting opportunities for future electronic applications.

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Data Availability Statement: Data available on request from the authors.

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