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Decoder-Type Scan Driver Suitable for Flexible and Stretchable Displays

Seo Jin Kang [ID], Hyuk Su Lee, Jae Geun Woo, Eun Seong Yu, Jong Mo Lee and Byung Seong Bae *[ID]

School of Electronics and Display Engineering, Hoseo University, Asan 31499, Korea;
kangseo4922@naver.com (S.J.K.); gur0545@daum.net (H.S.L.); wjg3802@gmail.com (J.G.W.);
kub2270@naver.com (E.S.Y.); jongmo@hoseo.edu (J.M.L.)
* Correspondence: bsbae3@hoseo.edu

Abstract: The integration of a scan drive circuit is required for flexible and stretchable displays because a rigid scan driver IC is not flexible and stretchable. In this study, decoder-type scan drivers were developed using amorphous IGZO thin-film transistors for both depletion and enhancement mode TFTs. Simulations and measurements show that the proposed decoder-type scan driver operates well for both the enhancement and depletion-mode TFTs without error. The measurement results show that the proposed circuit provides scan pulses well, even with depletion-mode TFTs with a large negative threshold voltage of around -25 V.

Keywords: scan driver; stretchable display; a-IGZO TFT; depletion mode

1. Introduction

Flat-panel displays such as liquid crystal display (LCD) and organic light-emitting diode (OLED) displays use a backplane with thin-film transistors (TFTs). Hydrogenated amorphous silicon (a-Si:H), low-temperature polycrystalline silicon (LTPS), and oxide TFTs are typically used for flat-panel displays [1–3]. To display images on a panel, display driver ICs (DDIs) are attached to a panel to interface with the electrical signals from image sources. A scan driver is used to select a horizontal line to write image data to pixels on a panel. In active-matrix displays, image data are written on a panel line by line. A scan driver selects a line to which image data are written [4].

The integration of the scan driver enables a narrow bezel and good reliability of the module. In addition, unlike a rigid scan driver IC, it is suitable for flexible displays with various form factors, or for stretchable displays that can be stretched like rubber. An integrated data drive circuit and scan driver has been developed, but due to high-level requirements, integrated scan drivers are mostly being used in LCD or OLED displays [5–7].

A typical scan driver is composed of a shift register, level shifter, and buffer. The shift register is a cascade of flip-flops and the output of a flip-flop is transferred to the input of the next flip-flop. An input start pulse to the first flip-flop of the shift register is shifted to the next flip-flop one by one, in sync with clocks. Each output is processed by a level shifter to turn TFTs on and off. Finally, a TFT of the pixel is turned on and off after increasing the driving ability by a buffer [8,9].

An inverter is a basic logic gate for designing a digital circuit, and CMOS inverters are widely used due to their high speed, low static current, and low power consumption. However, the use of a CMOS inverter is not possible with a-Si:H and oxide TFTs due to the absence of p-channel TFTs. Inverters with only n-channel TFTs show voltage loss, large static current, and offset voltage in a low output state [10]. To overcome these issues, several scan driver circuits have been proposed, including a scan driver with a-Si:H TFTs consisting of four TFTs and one capacitor [11]. In this circuit, the gate voltage of a drive TFT is bootstrapped when the output voltage increases to a high level. The gate voltage increased by bootstrapping reduces the voltage loss of the output pulse and increases the

current driving ability. However, when the scan output is low, the scan output node floats and is not connected to any voltage source. Therefore, the output is unstable during the off state, which deteriorates the image quality. Circuits that reduce the output noise were proposed which use clock signal coupling [12–14].

However, there is an issue to consider when implementing these circuits on a flexible display. Flexible displays are subjected to external mechanical stress, which induces electrical failure. Therefore, conventional scan drivers in which the output of a stage becomes the input of the next stage are not suitable for flexible displays because when a stage is faulty, all the subsequent stages become faulty as well [4].

There are studies on decoder-type scan drivers to simplify the conventional scan drive circuit and increase circuit stability. A decoder-type scan driver was proposed using a-Si:H TFTs [15], and improved by reducing the signal lines and area of the circuit [16]. A carry-free scan driver using a-IGZO oxide TFTs was also proposed. It was manufactured on a flexible PI substrate and showed stable operation even after the 10,000 cycles of a bending test with a bending radius of 2 mm [6]. However, oxide TFTs including a-IGZO TFT often exhibit depletion-mode characteristics which have a negative threshold voltage (Vth), and a negative shift of the Vth by light illumination and negative bias stress [17–25]. The band-gap states and adsorption of oxygen and water molecules were studied in terms of the stability of the oxide TFTs. The adsorption and desorption of the oxygen and water molecules onto the backchannel were found to affect the stability of oxide TFTs [25]. However, in the top-gate structure TFT used in this study, the gate insulator and the gate metal act as passivation layers. Therefore, in the top gate structure, band-gap states play an important role in the instability of the oxide TFTs. It is known that oxygen vacancy states below the Fermi level act as donors when ionized by light illumination, which is the reason for the large negative shift under illumination. Therefore, the control of the oxygen vacancy is important to control the threshold voltages of the oxide TFTs. The large amount of oxygen vacancy results in a depletion-mode TFT by the donor states generated by thermally ionized oxygen vacancies. Due to the depletion-mode characteristics of the a-IGZO TFT, many problems arise when driving a conventional gate drive circuit [26]. To solve this problem, many research groups have proposed gate drive circuits that can be operated with depletion-mode oxide TFTs [26–33].

In a circuit, leakage control is difficult with depletion-mode TFTs because the off state is not realized by zero gate bias with zero-volt ground. To turn off a depletion-mode TFT, the gate bias should be lower than the source and drain voltages. One circuit for a depletion-mode TFT uses multiple grounds with different voltages, and others use bootstrapping to shift the gate voltage to the negative and two series-connected transistors [28–33]. All these circuits require a design change when the mode of the TFT changes from enhancement mode to depletion mode. A circuit which is adaptive to both the enhancement and depletion modes can be used in any case without a design change.

In this work, a scan driver that can operate well for both the enhancement and depletion mode is proposed. The proposed circuit is evaluated by simulation and measurement. It is suitable for a flexible backplane of a display because of its small circuit area due to a reduced number of TFTs and decoder-type block driving. The proposed scan drive circuits are fabricated on a glass substrate using a-IGZO TFTs to verify their performance.

2. Proposed Scan Drivers

A unit stage of the proposed scan driver and its timing chart are shown in Figure 1a,b. When PS is high, TFT T1 is turned on and node P is charged with the high voltage of the PS signal, which turns on TFT T2. The scan output then becomes high when SS becomes high. Increase of the scan voltage bootstraps node P's voltage up using coupling capacitor C1. Bootstrapping the gate voltage of T2 reduces the threshold voltage loss of the scan output. The voltage of PS should be higher than SS by more than the threshold voltage in order to avoid output-voltage loss and low on current because $V_{gs} = V_g - V_s$ is given by $V_{PS} - V_{SS}$. Low Vgs results in a drop of the output voltage and long rise and fall times of the output

pulses. The bootstrapped gate voltage of the drive TFT reduces the rise time of the output pulse by increasing the current driving ability.
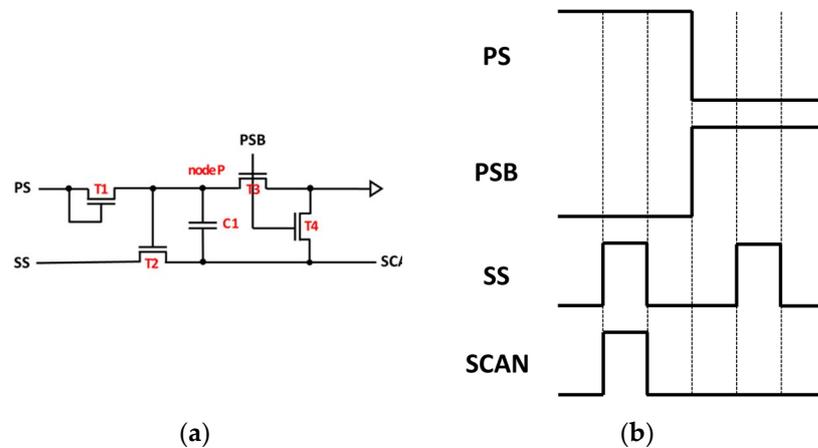

Figure 1. The unit stage (**a**) and timing chart (**b**) of the proposed scan driver.

When the scan output is high, TFTs T4 and T3 are turned off by PSB. When SS becomes low, the scan output becomes low. To avoid a floating state in the scan line, PSB becomes high when PS becomes low. When PS is low and PSB is high, T3 and T4 turn on. Then, node P is discharged to the ground level, and the scan is electrically connected to the ground level to avoid a floating state in the scan line.

The scan driver should provide sequential outputs to scan lines; Figure 2a shows its block diagram, and Figure 2b shows its timing chart. The driver consists of several blocks that use multiple SS signals; Figure 2a shows 30 SS signals. After the PS1 pulse becomes high, all the TFTs in block 1 turn on, and SS signals appear at the scan output sequentially from SS1 to SS30. Next, a PS2 pulse is applied to all the TFTs in block 2, which in turn output SSs from SS1 to SS30 sequentially. By adjusting the number N of SS pulses and the number M of blocks, we can scan M × N lines.
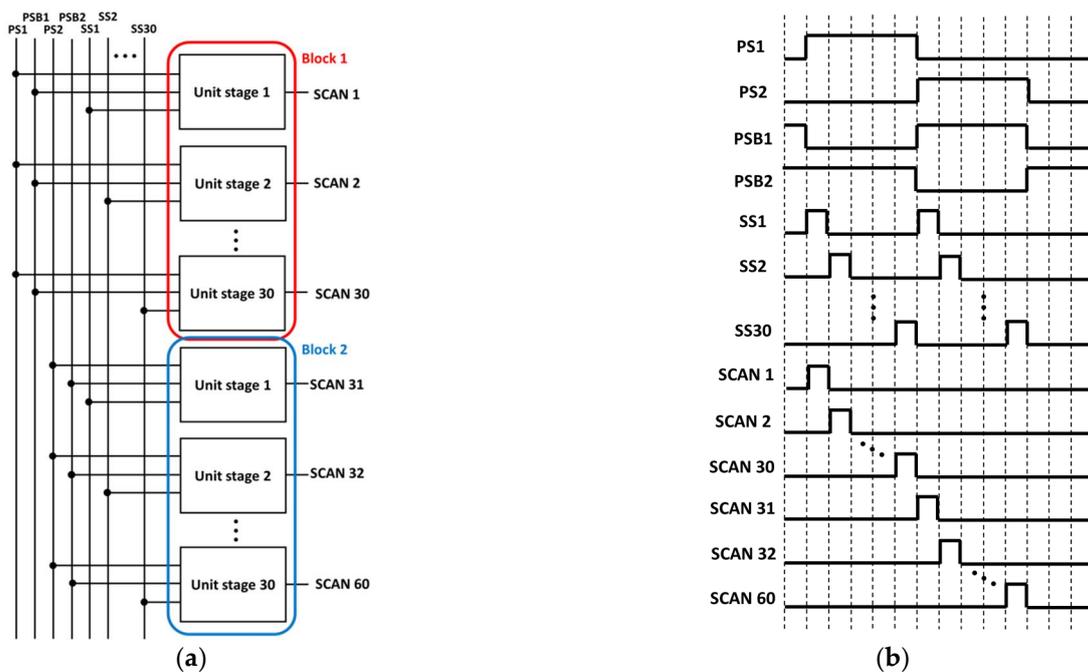

Figure 2. Block diagram of the proposed scan driver (**a**) and its timing chart (**b**).

Figure 3a shows simulation results for both the unit stage of the proposed scan driver and a scan driver with two switch TFTs, as shown in Figure 4. PS, PSB, and SS signals are shown, and the output pulses are shown at the lowest. The pulses from both the circuit in Figure 4 and the proposed one are shown and replotted in Figure 3b. Output voltages in Figure 3b show the effect of bootstrapping in the proposed circuit—the voltage loss was reduced for the proposed circuit. Increasing the gate voltage of the drive TFT by bootstrapping shortened the rise time and reduced the voltage drop in the output. Table 1 shows that the rise time decreased to 26.9 μs from 174.5 μs, and the ratio of the output voltage to SS increased from 0.863 to 0.999.
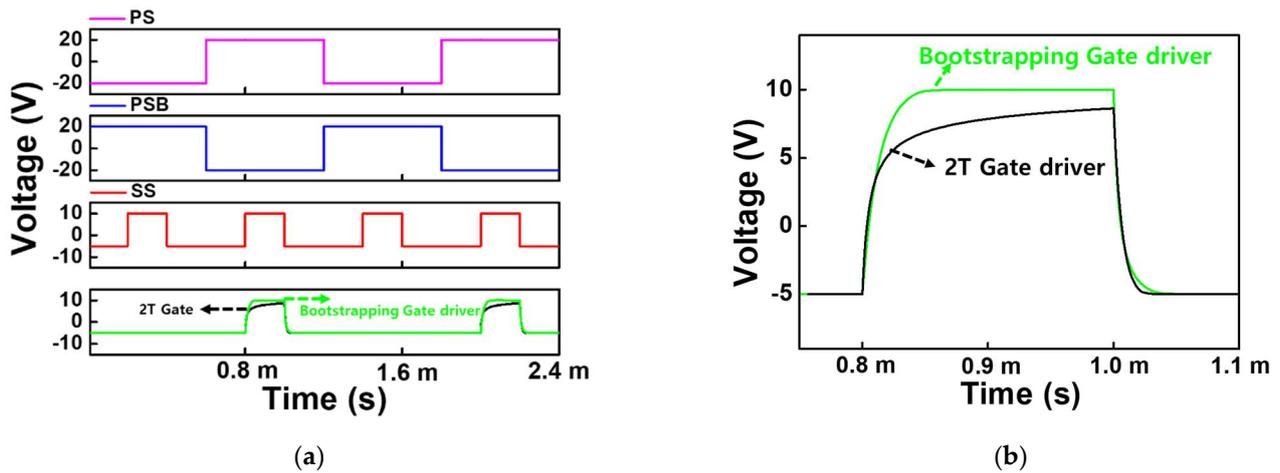

(a)   (b)

Figure 3. (**a**) Simulated waveforms for both the proposed circuit and 2TFT circuit; (**b**) comparison between two outputs.
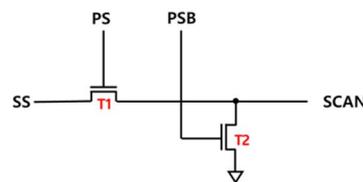

Figure 4. Unit scan drive circuit with two switch TFTs.

Table 1. Comparison of driving characteristics of the proposed circuit and 2TFT circuit.

	2T Scan Driver	**Proposed Scan Driver**
Rise time	174.5 μs	26.9 μs
Fall time	13.5 μs	15.6 μs
Ratio of output voltage to SS	0.863	0.999

The gate of TFT T1 in Figure 1a is connected to the drain electrode and acts as a diode. However, with a depletion-mode a-IGZO TFT, currents flow even in reverse bias because the off state cannot be accomplished with zero bias between the gate and drain. Therefore, currents flow even in reverse bias with the drain voltage lower than the source voltage. As a result, during the increase of the node P voltage by bootstrapping, current flows through T1, and bootstrapping does not occur.

To settle this issue, the gate and drain electrodes of T1 are separated as shown in Figure 5a. The timing chart is shown in Figure 5b. Unlike the previous bootstrapped circuit, the drain of T1 is not connected to the gate and is connected to Vpulse.
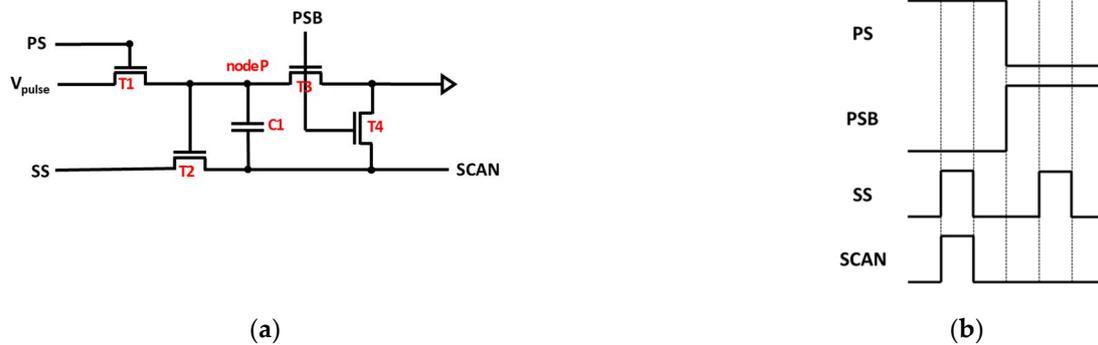
Figure 5. (**a**) Unit-stage modified bootstrap scan driver; (**b**) timing chart.

The operation of the modified bootstrap scan driver is shown in Figure 6. In the reset period, the PSB signal is high, and TFTs T3 and T4 are turned on. The scan line of the previous stage is initialized through TFT T4. In addition, since Vpulse is in a high state, a high voltage of Vpulse is charged in node P, which in turn turns on T2. In the output period, PS and Vpulse become high, which turns on TFTs T1 and T2. When SS becomes high in the output period, the scan output increases, which bootstraps the node P voltage through coupling capacitor C1. The PS low voltage should be lower than that of Vpulse to make T1 be in an off state, which enables the bootstrapping in node P by the low leakage of T1. The increased gate voltage of T2 by bootstrapping prevents voltage loss of the SS output to the scan line.
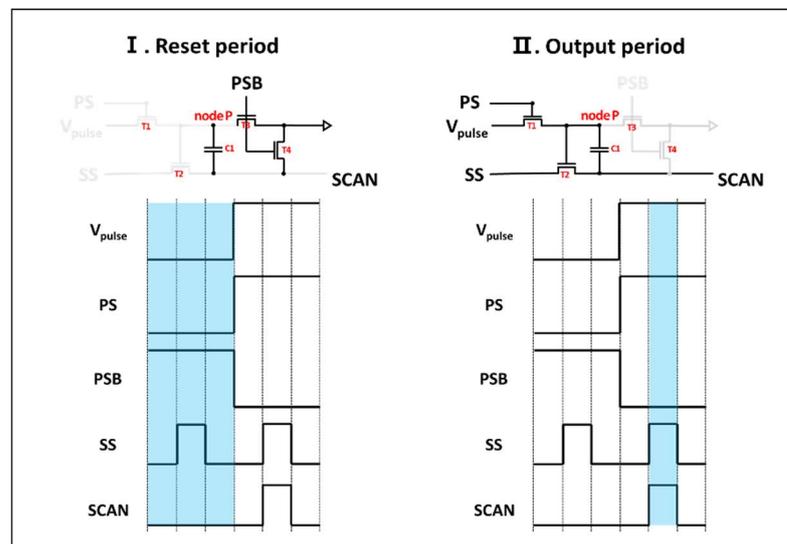

Figure 6. Operation of the modified bootstrap scan driver.

Figure 7 shows the transfer characteristics of the depletion-mode TFT. Figure 8a,b shows the simulation results from using parameters of the depletion-mode TFT as shown in Figure 7. Figure 8a shows the result for the proposed circuit shown in Figure 1a, and Figure 8b shows the result for the modified circuit shown in Figure 5a. The modified bootstrap circuit showed improved error-free driving capability because the current flowing through T1 during bootstrapping to the T2 gate was suppressed by applying the appropriate voltages of Vpulse and PS. Since one advantage of the proposed circuit is adaptive operation for both the enhancement and depletion-mode TFTs without design change, we verified the operation using enhancement-mode TFT parameters as shown in Figure 8c. We changed

the threshold voltage parameter to 20 V for the enhancement-mode simulation. Figure 8c shows the output waveforms without error. The rise time increased because the threshold voltage was large for the worst-case simulation.
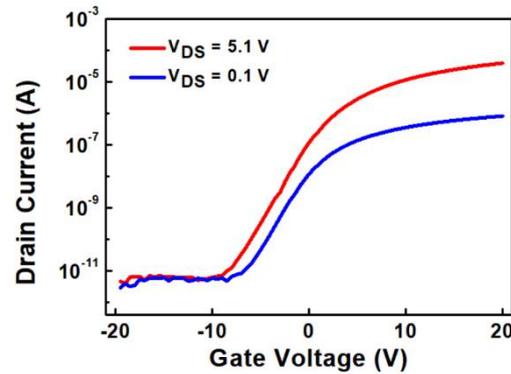

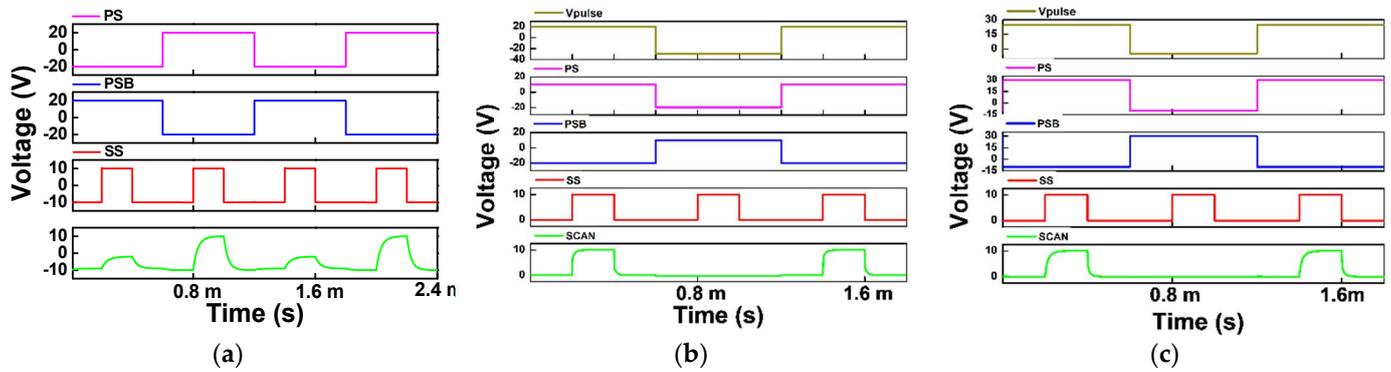**Figure 7.** Transfer characteristic of the depletion-mode TFT.

Figure 8. (**a**) Simulated waveforms for unit-stage bootstrap circuit using depletion-mode TFT; (**b**) simulated waveforms for the unit-stage modified bootstrap circuit using depletion-mode TFT; (**c**) simulated waveforms for unit-stage modified bootstrap circuit using enhancement-mode TFT.

Figure 9 shows a more detailed comparison between outputs for both the bootstrap circuit and modified bootstrap circuit. Improved results with the modified bootstrap scan driver are summarized in Table 2. The rise time decreased to 12.3 µs from 68.4 µs, and the fall time decreased to 10.9 µs from 60.5 µs.
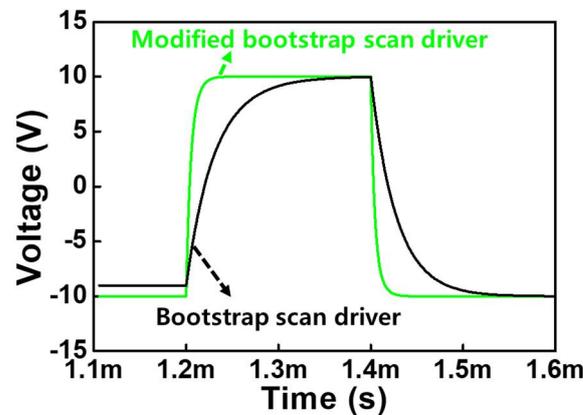

Figure 9. More detailed comparison between outputs for both the bootstrap circuit and modified bootstrap circuit.

Table 2. Comparison of driving characteristics of bootstrap scan driver and modified bootstrap scan driver.

	Bootstrap Scan Driver	Modified Bootstrap Scan Driver
Rise time	68.4 µs	12.3 µs
Fall time	60.5 µs	10.9 µs
Ratio of output voltage to SS	0.995	0.999

3. Materials and Methods

Drive circuits were fabricated using an a-IGZO TFT process on a glass substrate. The cross-sectional structure and a microscopic image of the top-gate a-IGZO TFT are shown in Figure 10a,b, respectively. A 50 nm-thick active layer of a-IGZO was deposited by RF magnetron sputtering with Ar gas mixed with O_2 gas (Ar:O_2 = 22.5 sccm:7.5 sccm) using an IGZO target (In_2O_3:Ga_2O_3:ZnO = 2:1:2 in mole ratio). The working pressure was 5 mTorr, and the power was 50 W.
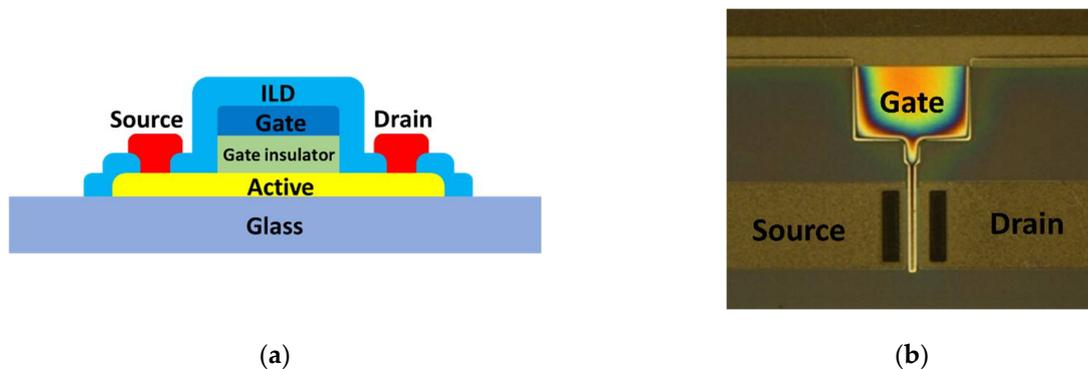

(**a**) (**b**)

Figure 10. (**a**) Cross-sectional structure of the top gate a-IGZO TFT used for the fabrication of the circuits; (**b**) microscopic view of the fabricated a-IGZO TFT.

After making a photoresist pattern by photolithography, the a-IGZO layer was etched by buffered oxide etchant (BOE) diluted with water at a 500:1 ratio to make an a-IGZO active pattern. A 500 nm-thick gate insulator was formed by spin-coating SU-8 negative photoresist, followed by a curing process. A 200 nm-thick Al layer was deposited by DC magnetron sputtering. The working pressure of Al sputtering was 5 mTorr in Ar gas, and the DC power was 250 W. After deposition of Al, it was wet-etched to form a gate electrode.

After the gate pattern, SU-8 insulator was removed except for the part under the gate electrode. This was done by reactive ion etching (RIE) with oxygen plasma, a flow rate of 60 sccm, and power of 180 W. During over-etching of the SU-8 insulator, the source and drain regions of IGZO were doped to achieve low sheet resistance. Then, 500 nm-thick SU-8 was formed for inter-layer dielectrics (ILDs) by spin-coating and curing. After contact hole etching by RIE, Al was deposited by DC magnetron sputtering and patterned by wet etching to form source and drain electrodes.

4. Results and Discussion

Figure 11 shows the transfer characteristics of the fabricated a-IGZO TFT with a channel width and length of 100 and 10 µm, respectively. The fabricated TFT showed negative shift in the transfer characteristics, which can be attributed to both the oxygen vacancies and the hydrogen ion in the SU-8 gate insulator. The oxygen vacancies act as donors when ionized by molecular vibration energy, which results in a negative shift of the threshold voltage by increased carrier density. The other factor explaining the negative shift is the hydrogen atom in the SU-8 gate insulator, because the hydrogen is believed to serve as a donor in the IGZO layer. The hydrogen ions are generated during UV illumination for curing the SU-8 negative photoresist. Therefore, the remaining hydrogen in SU-8 gate

insulator can diffuse into the IGZO interface, which results in the negative shift of the threshold voltage by increased carrier density.
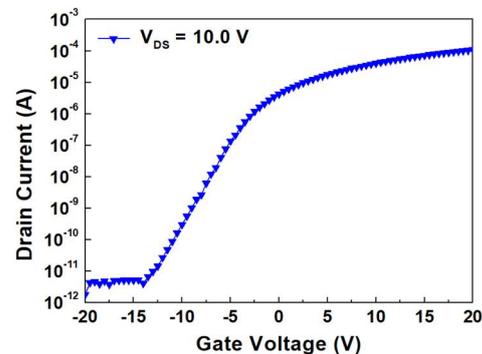

Figure 11. Transfer characteristics of the fabricated a-IGZO TFT.

Table 3 shows the parameters extracted from the fabricated a-IGZO TFT. The field-effect mobility and on/off ratio were 6.2 cm^2/V·s and 2.1 × 10^7, respectively. The sub-threshold swing was 1.8 V/dec, and the threshold voltage was −4.8 V. The mobility and threshold voltage were obtained from the saturation current (I_{ds}) Equation (1):

$$I_{ds} = \frac{1}{2}\frac{W}{L}\mu_{FE}C_{ox}\left(V_{gs} - V_{th}\right)^2 \tag{1}$$

where W and L are channel width and length, respectively. C_{ox} is the capacitance of the gate insulator per unit area and μ_{FE} is a field effect mobility. The subthreshold swing (SS) was obtained according to Equation (2).

$$SS = \left(\frac{dlog(I_{ds})}{dV_{gs}}\right)^{-1} \tag{2}$$

Table 3. The electrical parameters of the fabricated a-IGZO TFT.

a-IGZO TFT Parameters	Values
Mobility	6.2 cm^2/V·s
I_{ON}/I_{OFF} ratio	2.1 × 10^7
Subthreshold swing	1.8 V/dec
Threshold voltage	−4.8 V

Microscopic images of fabricated drivers are shown in Figure 12a,b. Figure 12a shows the bootstrap scan driver, and Figure 12b shows the modified bootstrap scan driver. The circuit area of a unit stage was 620 μm × 290 μm. The design parameters of the scan drivers are indicated in Table 4. In order to ensure driving capability, the size of the drive TFT, T2, was designed to be the largest among all four TFTs. T3 and T4 are TFTs for reset. The difference between Figure 12a,b is whether T1's gate is connected to the drain or not. In the modified bootstrap scan driver, the drain of T1 is not connected to the gate and is connected to Vpulse.

The measurement results of the bootstrap scan driver and modified bootstrap scan driver are shown in Figure 13 with waveforms of input signals. There were errors in the bootstrap scan driver's output waveform, while the modified bootstrap scan driver showed a good output waveform without errors. The modified bootstrap scan driver eliminated errors by appropriately adjusting the Vpulse signal connected to the drain of T1 and the PS signal connected to the gate of T1.
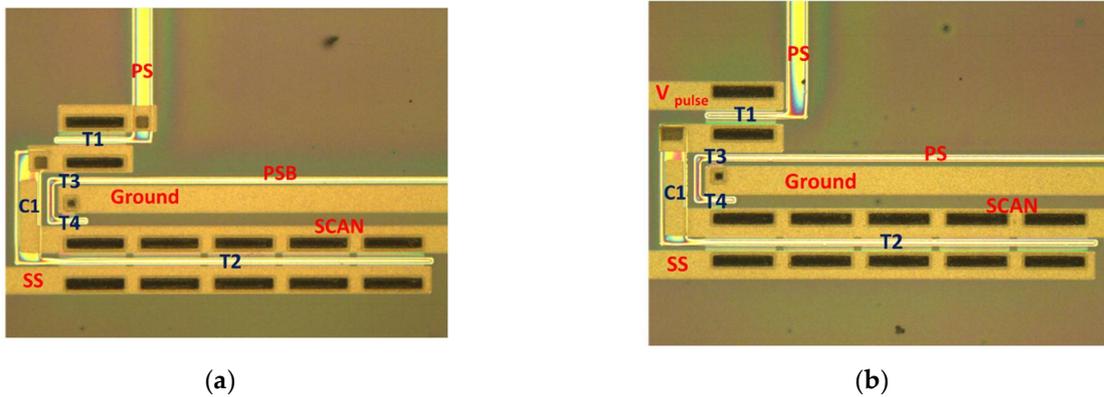
Figure 12. Microscopic image of the fabricated unit-stage drive circuits for the (**a**) bootstrap scan driver and (**b**) modified bootstrap scan driver.

Table 4. Design parameters of the bootstrapped scan driver and the modified bootstrapped scan driver.

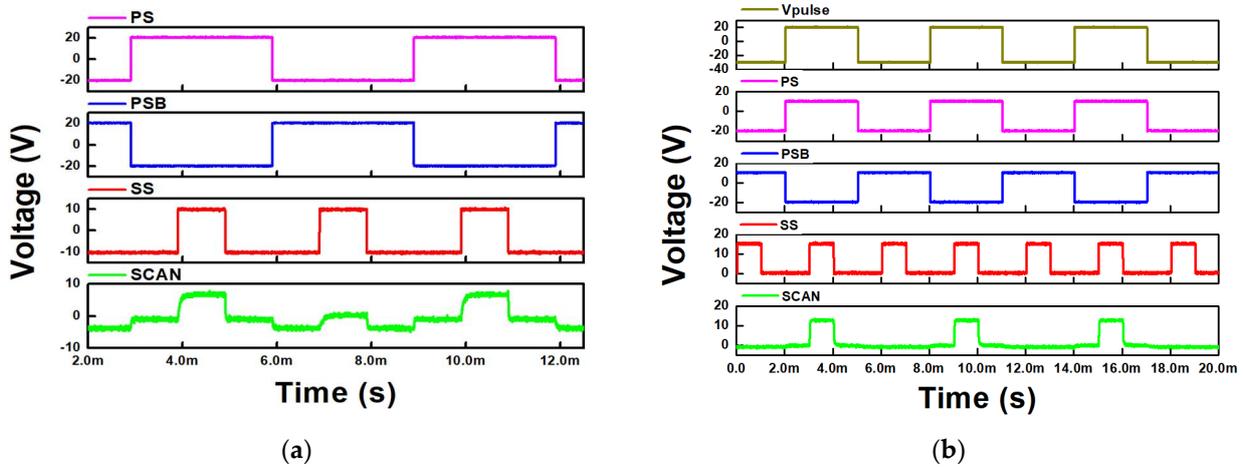| TFT	Width/Length
T1	100/10
T2	500/10
T3, T4	20/10
C1	0.2 pF

Figure 13. Measured waveforms of the fabricated single-stage drive circuits with TFTs are shown in Figure 10. (**a**) Bootstrap scan driver and (**b**) modified bootstrap scan driver.

Figure 14 shows the transfer characteristic, in which the threshold voltage was more negative than in Figure 10. Figure 15 shows the measured output waveform of scan drivers with the TFTs shown in Figure 14. Figure 15a,b shows the output waveforms of the bootstrap scan driver and modified bootstrap scan driver, respectively. The operation frequency was 1 kHz. Since the TFT used was more negatively shifted than the TFT in Figure 10, Figure 15a shows a larger error than Figure 13a. However, as shown in Figure 15b, the modified bootstrap scan driver showed no error.
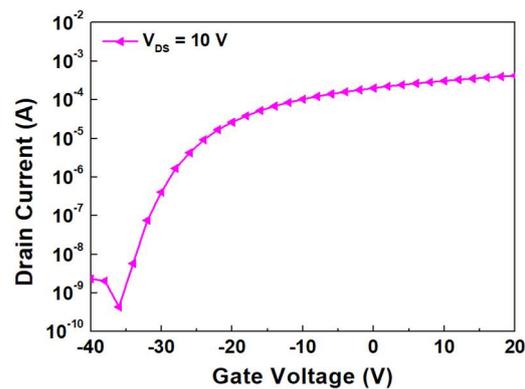
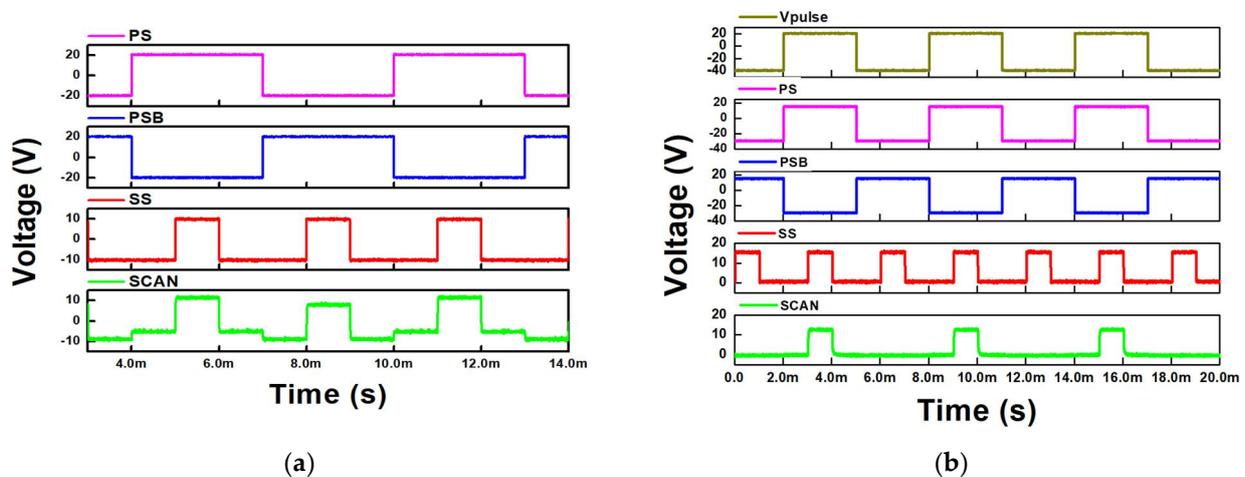**Figure 14.** Completely depletion-mode a-IGZO TFT transfer characteristics.

(**a**)　　　　　　　　　　　　　　　　　　　　　(**b**)

Figure 15. Measured waveforms of the fabricated single-stage drive circuits with the TFTs shown in Figure 14: (**a**) bootstrap scan driver; (**b**) modified bootstrap scan driver.

5. Conclusions

We proposed a decoder-type a-IGZO scan driver that is suitable for flexible and stretchable displays. Since a-IGZO TFTs often exhibit depletion-mode characteristics that have a negative threshold voltage (Vth), the proposed circuit was designed to operate well for both enhancement and depletion-mode TFTs. The circuits were optimized by a circuit simulation and fabricated by an a-IGZO TFT process. The simulation and measurement showed that the proposed decoder-type scan driver operated well for both the enhancement and depletion-mode TFTs without error. The operation at the threshold voltage of 20 V was verified by the simulation, and the measurement results showed that the proposed circuit provided scan output pulses with depletion-mode TFTs with a large negative threshold voltage of -25 V.

Author Contributions: S.J.K. and H.S.L.: Conceptualization, data curation, simulation and measurement, writing. J.G.W., E.S.Y. and J.M.L.: Experiment, measurement. B.S.B.: Conceptualization, writing, review, and editing. All authors have read and agreed to the published version of the manuscript.

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References

1. Park, J.S.; Maeng, W.J.; Kim, H.S.; Park, J.S. Review of Recent Developments in Amorphous Oxide Semiconductor Thin-Film Transistor Devices. *Thin Solid Films* **2012**, *520*, 1679–1693. [CrossRef]
2. Hsieh, H.H.; Lu, H.H.; Ting, H.C.; Chuang, C.S.; Chen, C.Y.; Lin, Y. Development of IGZO TFTs and Their Applications to Next-Generation Flat-Panel Displays. *J. Inf. Disp.* **2010**, *11*, 160–164. [CrossRef]
3. Ji, D.; Jang, J.; Park, J.H.; Kim, D.; Rim, Y.S.; Hwang, D.K.; Noh, Y.Y. Recent Progress in the Development of Backplane Thin Film Transistors for Information Displays. *J. Inf. Disp.* **2021**, *22*, 1–11. [CrossRef]
4. Ke, J.; Deng, L.; Zhen, L.; Wu, Q.; Liao, C.; Luo, H.; Huang, S. An AMOLED Pixel Circuit Based on LTPS Thin-film Transistors with Mono-Type Scanning Driving. *Electronics* **2020**, *9*, 574(1)–574(11). [CrossRef]
5. Wu, W.J.; Zhang, L.R.; Xu, Z.P.; Zhou, L.; Tao, H.; Zou, J.H.; Xu, M.; Wang, L.; Peng, J.B. A high-Reliability Gate Driver Integrated in Flexible AMOLED Display by IZO TFTs. *IEEE Trnans. Electron. Devices* **2017**, *64*, 1991–1996. [CrossRef]
6. Kim, J.S.; Byun, J.W.; Jang, J.H.; Kim, Y.D.; Han, K.L.; Park, J.S.; Choi, B.D. A High-Reliability Carry-Free Gate Driver for Flexible Displays Using a-IGZO TFTs. *IEEE Trnans. Electron. Devices* **2018**, *65*, 3269–3276. [CrossRef]
7. Kim, D.S.; Kwon, O.K. A small-Area and Low-Power Scan Driver Using a Coplanar a-IGZO Thin-Film Transistor With a Dual-Gate for Liquid Crystal Displays. *IEEE Electron. Device Lett.* **2017**, *38*, 195–198. [CrossRef]
8. Wu, W.J.; Chen, J.W.; Wang, J.S.; Zhou, L.; Tao, H.; Zou, J.H.; Xu, M.; Wang, L.; Peng, J.B.; Chan, M. High-Resolution Flexible AMOLED Display Integrating Gate Driver by Metal-Oxide TFTs. *IEEE Electron. Device Lett.* **2018**, *39*, 1660–1663. [CrossRef]
9. Saraf, A.; Tripathi, A.N. Performance Analysis of Gate Driver Circuit for TFT-LCD. *IJERT* **2014**, *3*, 43–46.
10. Reita, C. Integrated Driver Circuits for Active Matrix Liquid Crystal Displays. *Display* **1993**, *14*, 104–114. [CrossRef]
11. Kim, T.W.; Park, G.T.; Choi, B.D.; Hong, M.P.; Jang, J.N.; Song, B.C.; Lee, D.H.; Bae, B.S. Decoder-Type Gate Driver Circuits Fabricated with Amorphous Silicon Thin-Film Transistors for Active Matrix Displays. *Jpn. J. Appl. Phys.* **2011**, *50*, 03CC03(1)–03CC03(8).
12. Maurice, F.; Lebrun, H.; Szydlo, N.; Rossini, U.; Chaudet, R. High Resolution Projection Valve with the Amorphous Silicon AMLCD Technology. *Proj. Disp. IV* **1998**, *3296*, 92–99.
13. Oh, J.H.; Hur, J.H.; Son, Y.D.; Kim, K.M.; Kim, S.H.; Kim, E.H.; Choi, J.W.; Hong, S.M.; Kim, J.O.; Bae, B.S.; et al. 2.0 inch a-Si:H TFT-LCD with Low Noise Integrated Gate Driver. *SID Int. Symp. Dig. Tech. Pap.* **2005**, *36*, 942–945. [CrossRef]
14. Chu, L.W.; Liu, P.T.; Ker, M.D. Design of Integrated Gate Driver with Threshold Voltage Drop Cancellation in Amorphous Silicon Technology for TFT-LCD Application. *J. Display Technol.* **2011**, *7*, 657–664. [CrossRef]
15. Kim, J.S.; Park, G.T.; Kim, H.W.; Choi, B.D. Compact Decoder-Type Gate Driver Circuits with Hydrogenated Amorphous Silicon Thin Film Transistors for Active Matrix Displays. *Jpn. J. Appl. Phys.* **2013**, *52*, 03BC01(1)–03BC01(5). [CrossRef]
16. Kim, J.S.; Choi, B.D. A New Decoder-Type Integrated Gate Driver with a-Si:H TFTs for Active-Matrix Displays. *Jpn. J. Appl. Phys.* **2014**, *53*, 03CD03(1)–03CD03(7). [CrossRef]
17. Son, K.S.; Kim, T.S.; Jung, J.S.; Ryu, M.K.; Park, K.B.; Yoo, B.W.; Park, K.C.; Kwon, J.Y.; Lee, S.Y.; Kim, J.M. Threshold Voltage Control of Amorphous Gallium Indium Zinc Oxide TFTs by Suppressing Back-Channel Current. *Electrochem. Solid-State Lett.* **2009**, *12*, H26–H28. [CrossRef]
18. Lee, K.W.; Shin, H.S.; Heo, K.Y.; Kim, K.M.; Kim, H.J. Light Effects of the Amorphous Indium Gallium Zinc Oxide Thin-Film Transistor. *J. Inf. Display* **2009**, *10*, 171–174. [CrossRef]
19. Lee, K.H.; Jung, J.S.; Son, K.S.; Park, J.S.; Kim, T.S.; Choi, R.; Jeong, J.K.; Kwon, J.Y.; Koo, B.W.; Lee, S.Y. The Effect of Moisture on the Photon-Enhanced Negative Bias Thermal Instability in Ga-In-Zn-O Thin Film Transistors. *Appl. Phys. Lett.* **2009**, *95*, 232106-1–232106-3. [CrossRef]
20. Lee, K.M.; Oh, M.S.; Mun, S.J.; Lee, K.H.; Ha, T.W.; Kim, J.H.; Park, S.H.K.; Hwang, C.S.; Lee, B.H.; Sung, M.M.; et al. Interfacial Trap Density-of-States in Pentacene- and ZnO-Based Thin-Film Transistors Measured via Novel Photo-Excited Charge-Collection Spectroscopy. *Adv. Mater.* **2010**, *22*, 3260–3265. [CrossRef]
21. Oh, H.C.; Yoon, S.M.; Ryu, M.K.; Hwang, C.S.; Yang, S.H.; Park, S.H.K. Photon-Accelerated Negative Bias Instability Involving Subgap States Creation in Amorphous In-Ga-Zn-O Thin Film Transistor. *Appl. Phys. Lett.* **2010**, *97*, 183502(1)–183502(3). [CrossRef]
22. Yang, B.S.; Huh, M.S.; Oh, S.H.; Lee, U.S.; Kim, Y.J.; Oh, M.S.; Jeong, J.K.; Hwang, C.S.; Kim, H.J. Role of ZrO2 Incorporation in the Suppression of Negative Bias Illumination-Induced Instability in Zn–Sn–O Thin Film Transistors. *Appl. Phys. Lett.* **2011**, *98*, 122110(1)–122110(3). [CrossRef]
23. Ji, K.H.; Kim, J.I.; Jung, H.Y.; Park, S.Y.; Choi, R.; Kim, U.K.; Hwang, C.S.; Lee, D.S.; Hwang, H.S.; Jeong, J.K. Effect of High-Pressure Oxygen Annealing on Negative Bias Illumination Stress-Induced Instability of InGaZnO Thin Film Transistors. *Appl. Phys. Lett.* **2011**, *98*, 103509(1)–103509(3). [CrossRef]
24. Chen, T.C.; Chang, T.C.; Hsieh, T.Y.; Lu, W.S.; Jian, F.Y.; Tsai, C.T.; Huang, S.Y.; Lin, C.S. Investigating the Degradation Behavior Caused by Charge Trapping Effect under DC and AC Gate-Bias Stress for InGaZnO Thin Film Transistor. *Appl. Phys. Lett.* **2011**, *99*, 022104(1)–022104(3). [CrossRef]
25. Abliz, A.; Wan, D.; Duan, H.; Yang, L.; Mamat, M.; Chen, H.; Xu, L. Low-Frequency Noise in High Performance and Stability of Li-Doped ZnO Thin-Film Transistors. *J. Phys. D Appl. Phys.* **2020**, *53*, 415110(1)–415110(8). [CrossRef]
26. Kim, B.; Ryoo, C.I.; Kim, S.J.; Bae, J.U.; Seo, H.S.; Kim, C.D.; Han, M.K. New Depletion-Mode IGZO TFT Shift Register. *IEEE Electron. Device Lett.* **2011**, *32*, 158–160. [CrossRef]

27. Kim, J.H.; Oh, J.S.; Park, K.C.; Jeon, J.H.; Kim, Y.S. IGZO TFT Gate Driver Circuit with Improved Output Pulse. *IEEE J. Electron. Devices Soc.* **2018**, *7*, 309–314. [CrossRef]

28. Kim, B.; Choi, S.C.; Lee, S.Y.; Huk, S.H.; Jang, Y.H.; Kim, C.D.; Han, M.K. A Depletion-Mode a-IGZO TFT Shift Register with a Single Low-Voltage-Level Power Signal. *IEEE Electron. Device Lett.* **2011**, *32*, 1092–1094. [CrossRef]

29. Song, E.J.; Kang, B.U.; Han, I.H.; Oh, K.W.; Kim, B.S.; Nam, H.S. Depletion Mode Oxide TFT Shift Register for Variable Frame Rate AMOLED Displays. *IEEE Electron. Device Lett.* **2015**, *36*, 247–249. [CrossRef]

30. Kim, J.H.; Oh, G.S.; Park, K.C.; Kim, Y.S. IGZO TFT Gate Driver Circuit with Large Threshold Voltage Margin. *Displays* **2018**, *53*, 1–7. [CrossRef]

31. Oh, J.S.; Jung, K.M.; Lee, J.W.; Jung, E.K.; Jeon, J.H.; Park, K.C.; Kim, Y.S. A Novel Gate Driver Circuit for Depletion-Mode a-IGZO TFTs. *J. Soc. Inf. Display* **2019**, *27*, 776–784. [CrossRef]

32. Oh, J.S.; Jung, K.M.; Jung, E.K.; Lee, J.W.; Lee, S.Y.; Park, K.C.; Jeon, J.H.; Kim, Y.S. Novel Driving Methods of Gate Driver for Enhancement- and Depletion-Mode Oxide TFTs. *IEEE J. Electron. Devices Soc.* **2020**, *8*, 67–73. [CrossRef]

33. Kang, C.K.; Park, Y.S.; Park, S.I.; Mo, Y.G.; Kim, B.H.; Kim, S.S. Integrated Scan Driver with Oxide TFTs Using Floating Gate Method. *SID'11 Tech. Digest* **2011**, *42*, 25–27. [CrossRef]