Taylor & Francis
Taylor & Francis Group

Journal of Information Display

ISSN: (Print) (Online) Journal homepage: https://www.tandfonline.com/loi/tjid20

Effect of the spin-on-glass curing atmosphere on In–Ga–Zn–O thin-film transistors

Yeong Jo Baek , Eui-Jung Yun & Byung Seong Bae

To cite this article: Yeong Jo Baek , Eui-Jung Yun & Byung Seong Bae (2020) Effect of the spin-on-glass curing atmosphere on In–Ga–Zn–O thin-film transistors, Journal of Information Display, 21:4, 229-234, DOI: 10.1080/15980316.2019.1710586

To link to this article: https://doi.org/10.1080/15980316.2019.1710586

Published online: 07 Jan 2020.

JOURNAL OF INFORMATION DISPLAY
2020, VOL. 21, NO. 4, 229–234
https://doi.org/10.1080/15980316.2019.1710586

Taylor & Francis
Taylor & Francis Group

Effect of the spin-on-glass curing atmosphere on In–Ga–Zn–O thin-film transistors

Yeong Jo Baek[a], Eui-Jung Yun[b] and Byung Seong Bae[a]

[a]School of Electronics & Display Engineering, Hoseo University, Asan City, Republic of Korea; [b]Department of ICT Automotive Engineering, Hoseo University, Dangjin City, Republic of Korea

ABSTRACT

A solution-based spin-on glass (SOG) was applied to the gate insulator of an oxide thin-film transistor (TFT). The curing atmosphere of the SOG was investigated to enhance the performance of the self-aligned top-gate In–Ga–Zn–O (IGZO) TFT. After the SOG layer was formed on an IGZO active layer, curing was performed under N_2, air, and O_2 atmospheres. The curing under an N_2 atmosphere resulted in the best device characteristics for the IGZO TFT. After curing, the SOG films were investigated via atomic force microscopy, secondary ion mass spectroscopy, Fourier transform infrared spectroscopy, and capacitance measurement. The results showed that the N_2 pile-up at the back surface of the SOG is the main reason for the enhanced performance of the TFT after curing under an N_2 atmosphere.

ARTICLE HISTORY
Received 24 October 2019
Accepted 14 December 2019

KEYWORDS
Thin-film transistors; oxide semiconductor; spin-on glass; gate insulator; curing atmosphere

1. Introduction

Spin-on glass (SOG) is mainly used as an intermetal dielectric in semiconductor devices [1,2]. SOG is an insulator supplied in liquid form as a silicate polymer with an Si–O structure in an alcohol solvent system. It can be coated in a variety of ways, such as via spin coating, dipping, spraying, and printing [3,4]. After coating, it is cured in a furnace to form an SiO_2 layer. The sol–gel solution process has the advantages of planarization, low cost, and low process time compared with the vacuum process.

There are two types of SOG: inorganic silicate-based SOG and organic siloxane-based SOG. Siloxane-based SOG, which contains CH_3 or C_2H_5 with an Si–O bond, has higher viscosity and shows higher planarity than the other SOG types [3,5]. SOG has been studied as an insulator for thin-film transistors (TFTs) and flexible and large area electronics, but there have not been many studies on the use of SOG as a gate insulator in TFTs, especially oxide TFTs [6–11]. The dilution of SOG using 2-propanol and deionized (DI) water was reported to reduce the curing temperatures, and curing at 200 °C was tested [6]. The dilution of SOG by DI water was also reported to be applied to a metal insulator diode, and curing of SOG was performed at a temperature as low as 200 °C; [7].

An SOG gate insulator was applied for the gate insulator of bottom-gate polycrystalline silicon, and the effect of planarization on the gate electrode was reported [8]. Also, the application of the SOG gate insulator was reported for both the ZnN and a-SiGe TFTs [9,11]. Even though several solution-based materials have been evaluated for TFTs, the SOG gate insulator is rarely applied to oxide TFTs [10,12].

In this study, siloxane-based SOG was used for the gate insulator and interlayer dielectric in self-aligned top-gate amorphous In–Ga–Zn–O (IGZO) TFTs. Figure 1 shows the structure of the top-gate TFT studied in this paper. The top-gate TFT has a low parasitic capacitance due to the reduced overlap between the gate and the source/drain. Another advantage is that the active layer is protected from atmospheric impurities like hydrogen and moisture [13].

Device processes like annealing are generally performed under an N_2 atmosphere [2,4,14–16]. For certain processes, the annealing environment is a significant parameter that determines the device characteristics. Therefore, it is important to reveal the effect of the curing atmosphere on the SOG and TFT performance. The effect of the annealing ambient atmosphere (O_2, N_2, air, etc.) on the bottom-gate IGZO TFT with an SOG

CONTACT Byung Seong Bae bsbae3@hoseo.edu School of Electronics & Display Engineering, Hoseo University, Asan City, Chungnam 31499, Republic of Korea

ISSN (print): 1598-0316; ISSN (online): 2158-1606

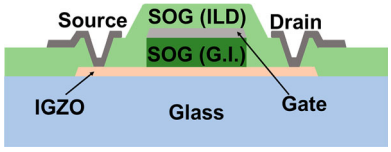

Figure 1. Cross-sectional structure of the fabricated top-gate IGZO TFTs using SOG as a gate insulator (GI) and an interlayer dielectric (ILD).

passivation layer has been reported, and the best performance was obtained when annealing was performed under an N_2 ambient atmosphere [17]. This study considered the effects of the curing atmosphere during the gate insulator process of SOG on the performance of an oxide TFT. The N_2, O_2, and air atmospheres were investigated.

2. Experiment

The oxide TFT was developed with siloxane-based SOG, which was used for both the gate insulator and the interlayer dielectric in the experiment. The gate electrode was Cr, and the source/drain was Al. The TFTs were fabricated on a glass substrate via photolithography, as shown in Figure 1. After cleaning the glass substrate, a 50-nm-thick IGZO active layer was deposited thereon at 250°C via RF magnetron sputtering using a target with a 1:1:1 In:Ga:Zn atomic ratio, under the following conditions: 50 W RF power, 0.7 Pa working pressure, and $Ar:O_2 = 25:7.5$ flow ratio. The IGZO layer was patterned via wet etching with a buffered-oxide-etch (BOE) solution diluted with DI water at a 500:1 ratio. After the IGZO patterning, the IGZO layer was annealed at 250°C for 1 h under an O_2 atmosphere to reduce the oxygen vacancies and the process-related defects. For the gate insulator on the IGZO layer, the SOG solution (Cospeen-1225G from NEPES) without dilution was spin-coated at 3000 rpm and soft-baked at 80°C for 1 min, followed by baking at 180°C for 1 min. After the soft baking, final curing was done to obtain a 360-nm-thick SOG gate insulator by increasing the temperature from 150°C to 450°C in 100°C intervals (the curing was performed for 15 min at 150, 250, 350, and 450°C, respectively). A 75-nm-thick Cr layer was deposited for the gate electrode via DC magnetron sputtering, and was patterned via wet etching. The gate insulator was etched via reactive ion etching (RIE), with the gate electrode used as an etching mask. The RF power, etching time, and working pressure were 180 W, 270 s, and 13.3 Pa, respectively. CF_4 and O_2 were used as the etching gases, and the $CF_4:O_2$ gas mixing ratio was 60:20. After etching the gate insulator, IGZO was doped via O_2 plasma treatment at room temperature for 30 s in an RIE chamber, under the following process conditions: 180 W RF power, 60 sccm O_2 flow, and 13.3 Pa working pressure. After doping, a 360-nm-thick SOG interlayer dielectric layer was formed via spin coating and curing, under the same conditions as those for the gate insulator. For the source/drain contact, a contact hole was formed in the interlayer dielectric. Before the contact hole patterning, oxygen plasma treatment under the same conditions as those for the doping was carried out to make the SOG surface hydrophilic. After performing contact hole dry etching for 170 s under the same conditions as those for the gate insulator etching, 75-nm-thick source and drain Al was deposited via DC magnetron sputtering, and was patterned via wet etching. The channel width and length of the fabricated TFTs were 40 and 20 μm, respectively.

The electrical characteristics of the fabricated TFTs were measured in a dark box to avoid light illumination instability. In addition to electrical characterization, the surface roughness of the SOG film was analyzed for various curing conditions via atomic force microscopy (AFM). Fourier transform infrared spectroscopy (FTIR) was used for investigating the bonding state, and secondary ion mass spectrometry (SIMS) was used for obtaining the depth profile of the N_2 concentration in the SOG film. For the above analyses, the SOG film was formed on a bare silicon wafer. The leakage current through the SOG layer was measured using a metal–insulator–metal (MIM) device with an Al–SOG–ITO structure.

3. Results and discussion

All the three kinds of IGZO TFT with different SOG gate insulator curing conditions were prepared for analyzing the electrical characteristics. The transfer characteristics of the TFTs were measured at a 10 V drain-to-source voltage (V_{DS}). Figure 2(a) shows the transfer characteristics of the IGZO TFTs with SOG gate insulators cured in N_2, air, and O_2 atmospheres. The effects of the dilution of SOG are shown in Figure 2(b), in which the mobility was shown to have been improved by the dilution of SOG [10]. As the gate insulator was formed from a non-diluted SOG solution, the mobilities were less than those of the TFTs with gate insulators obtained from the diluted SOG. The graph, however, clearly shows the effects of the different curing atmospheres. The on-currents and subthreshold slopes depended on the curing conditions, and the best performance was obtained for the TFT with an SOG gate insulator cured under a N_2 atmosphere.

The IGZO TFTs with SOG annealed under an N_2 atmosphere had the best electrical characteristics, as shown in Figure 2(a). This shows that N_2 plays a positive

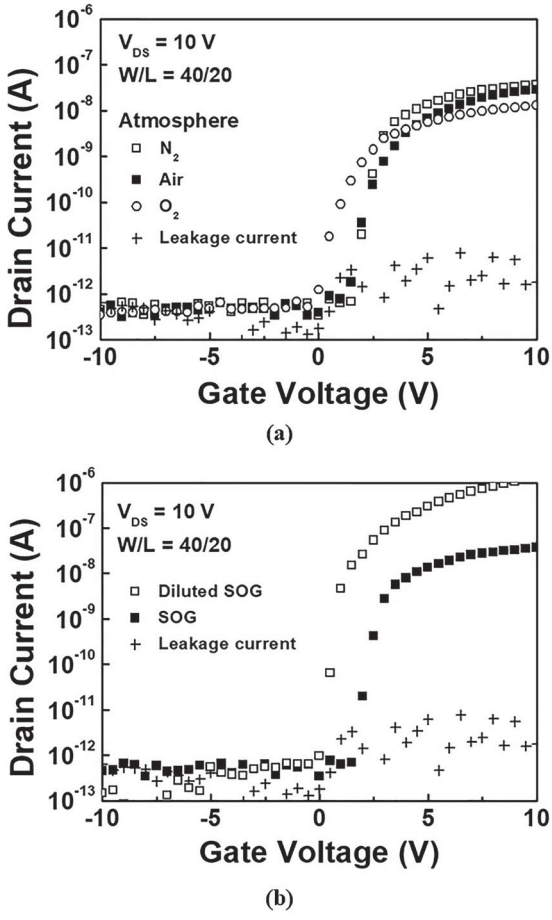

Figure 2. Transfer characteristics of the IGZO TFTs: (a) with different SOG curing atmospheres (N_2, air, and O_2) and (b) with diluted SOG curing in an N_2 atmosphere.

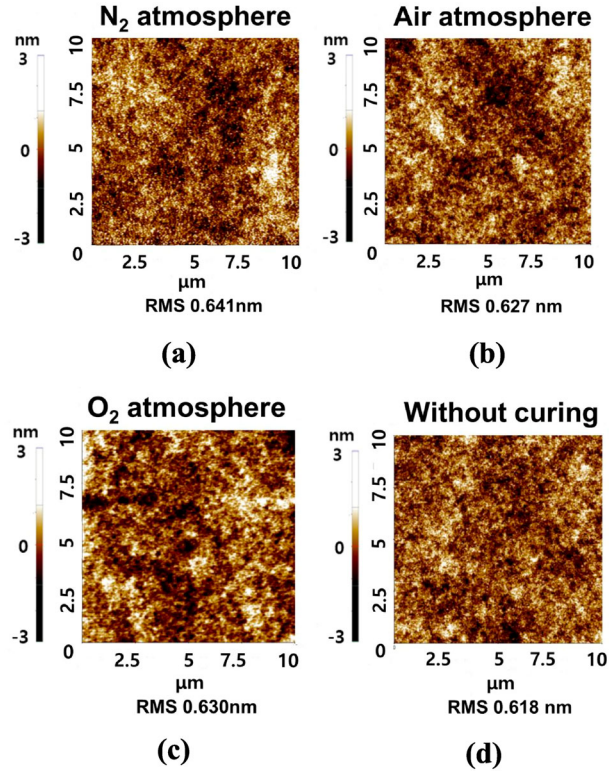

Figure 3. After the coating of a silicon wafer with the SOG films, the surface roughness was measured via AFM for various curing conditions: (a) N_2 atmosphere; (b) air atmosphere; (c) O_2 atmosphere; and (d) without curing.

role in determining the TFT characteristics. Several factors can affect the TFT characteristics, such as the surface state of the gate insulator, the states in the semiconductor layer, and the interface state between the gate insulator and semiconductor layers. A gate insulator with a rough surface causes low mobility due to the increase in carrier scattering at the surface [18]. As such, AFM analysis was performed to investigate the surface roughness of the SOG gate insulator. The SOG film formed on a bare silicon wafer was used for the AFM as well as for the FTIR and SIMS. Figure 3 shows the root mean square (RMS) roughness of the SOG gate insulator in each annealing atmosphere. The RMS value of the SOG without curing was 0.618 nm while that of the SOG cured in N_2, O_2, and air atmospheres were 0.641, 0.630, and 0.627 nm, respectively. The RMS values before and after the curing showed a very small change (about 0.02 nm). This suggests that the annealing atmosphere does not affect the surface roughness and is not a major factor in determining the TFT characteristics.

Figure 4 shows the FTIR absorption spectra of SOG thin films on a bare silicon wafer annealed under N_2, O_2, and air atmospheres. There were five major absorption peaks in the 400–1400 cm^{-1} range. The absorption peaks at 810 and 1130 cm^{-1} were assigned to the Si–N and Si–NH bonds, respectively [19,20]. One absorption peak at 1036 cm^{-1} was related to the Si–O–Si bonds while two peaks at 438 and 1274 cm^{-1} were assigned to the Si–O bonds [20–22]. The SOG thin films have an Si–O network, as evidenced by Figure 4. The Si–N bond peak at 810 cm^{-1} and the Si–NH bond peak at 1130 cm^{-1} were related to the amount of N_2 in the SOG, and had the largest intensity when annealed in an N_2 atmosphere. This can be attributed to the diffusion of a large amount of N_2 into the SOG during curing.

To explore the effect of N_2 on the dielectric constant and leakage currents of SOG thin films, the capacitances and leakage currents were measured for the MIM sample with an Al/SOG/ITO structure on a glass substrate. A larger capacitance of the gate dielectric layer improves the characteristics of TFTs through the larger induced channel charge due to the gate voltage [23,24]. As shown in Figure 5(a), the capacitances of all the samples were almost the same, suggesting that there is no significant

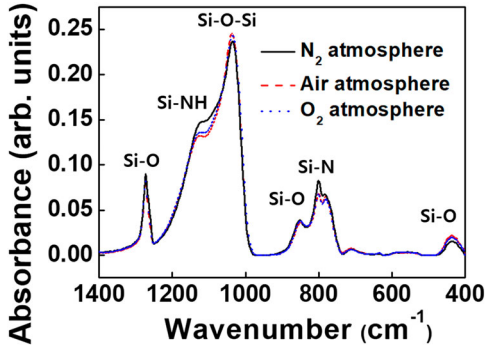

Figure 4. Infrared absorbance spectra of the SOG films on a bare silicon wafer. The spectra were obtained for various curing conditions (N_2, air, and O_2 atmospheres). The N_2-related bonds increased for the sample cured in an N_2 atmosphere.

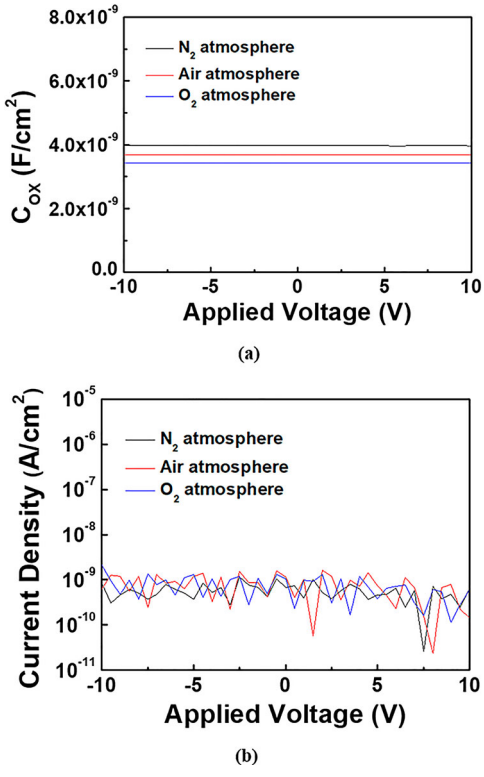

Figure 5. Measured capacitances (a) and leakage currents (b) for the MIM sample with an Al/SOG/ITO structure on a glass substrate. The dielectric properties were nearly the same, and the leakage currents were sufficiently low for TFT applications.

change in the dielectric constant of the SOG after curing in various atmospheres. Therefore, the annealing of SOG in various atmospheres hardly changes the dielectric properties of the SOG, which plays a small role in determining the electrical properties of TFTs. Figure 5(b) shows the leakage currents of the SOG thin films in this study, which were very small for all the three atmospheres. This suggests that the SOG gate insulators are good-quality insulators.

The N_2 depth profile was measured via SIMS for the SOG films on a silicon wafer, as shown in Figure 6. The SIMS depth profiles showed the N_2 depth profile from the front surface of the SOG film to the back surface, which was the interface with a silicon wafer. In the samples annealed under an N_2 atmosphere, a much higher N_2 concentration was observed at the interface between the SOG and the Si substrate as well as in the SOG film itself. This supports the excellent electrical properties obtained at the IGZO TFTs cured with N_2. The SIMS results showed that N_2 diffuses into the SOG layers and piles up at the SOG/IGZO interface during curing under an N_2 atmosphere, which means that N_2 atoms can diffuse into the IGZO layer and affect the electrical properties of the IGZO TFTs. In the case of the O_2 atmosphere, N_2 was detected even when the concentration was lowest at the bulk compared to those in the N_2 and air atmospheres. It is speculated that the remaining N_2 in the furnace diffused during the flow of O_2. At the interface, the N_2 concentration was higher than that for the air atmosphere, which shows the reversed distribution of N_2 at the interface over the bulk. More discussion and research are thus required. In general, the objective of N_2 doping in oxide semiconductors is to passivate the oxygen vacancy defects because the metal (Ga, In, Zn) can easily react with N_2. Therefore, N_2 occupies the oxygen vacancy sites, which results in less oxygen vacancies and better electrical performance of TFTs [25,26]. The in-situ incorporation of N_2 during the sputtering of IGZO was also reported to have enhanced the performance of the IGZO TFT [27]. The SIMS data showed that the N_2 concentration in the SOG film was the highest in the case of N_2 curing. Also, the N_2 atoms diffuse and reach the back surface during curing. The SIMS data in Figure 6 show that the N_2 atoms were piled up near the back surface, and that the highest N_2 concentration was obtained with N_2 curing. As shown in Figure 6, similar N_2 concentrations were observed near the surfaces of the SOGs, regardless of the ambient gases. This was attributed to the surface effect determined via SIMS analysis resulting from the fact that the outer surface reacts actively with the elements of the air and that the surface is a region whose SIMS profile is not reliable.

As diffused atoms exist as interstitial atoms or at the vacancy site, a higher concentration at the back surface means that the interface between the SOG and the Si wafer should be improved to reduce the vacancy and any other defect site that piles up with N_2. The SIMS data showed that N_2 could diffuse into the IGZO layer through the SOG layer in the top-gate IGZO TFT. The larger defect states at the interface usually result in the piling up of the diffused elements. It has been reported that the F concentration is higher at the interface due to the defects

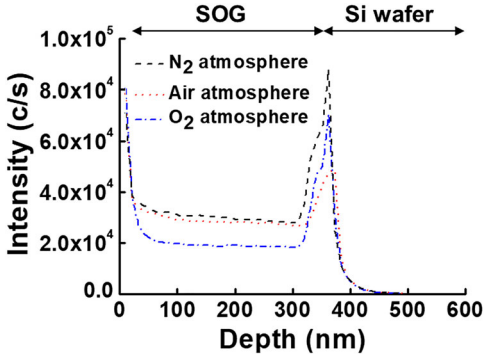

Figure 6. SIMS analysis results of the N2 depth profiles of the SOG films formed on Si wafer in various curing atmospheres. The profile shows that the N2 atoms piled up near the back surface and that the highest N2 concentration was obtained for N2 curing.

existing therein [28]. The field effect mobility, threshold voltage, and subthreshold swing of the TFTs annealed under an N_2 ambient atmosphere were 1.64 $cm^2/V{\cdot}s$, 1.82, and 0.36 V/dec, respectively. As N_2 atoms can create a bond with dangling bonds, such as oxygen vacancies, the increase in N_2 concentration at the back surface suggests that the concentration of defects near the back surface is much larger than that inside the SOG due to the formation of the lattice mismatch with the underlayer near the back surface. In the case of N_2 annealing, the 1.64 $cm^2/V{\cdot}s$ mobility and the 0.35 V/dec subthreshold swing were the best compared to 1.32 $cm^2/V{\cdot}s$ and 0.65 V/dec for air annealing and 0.47 $cm^2/V{\cdot}s$ and 0.50 V/dec for O_2 annealing. This can be explained by the following argument: the largest N_2 concentration inside the SOG for N_2 annealing, as shown in Figure 6, can cause the lowest number of defects inside the SOG due to the passivation of the oxygen-deficient sites by the N_2 atoms, indicating that the TFTs annealed under an N_2 ambient atmosphere had the best device properties. Therefore, the increased N_2 concentration near the back interface originated from the passivation of the defect states, which reduce the scattering of the carrier at the interface, leading to an increase in the field effect mobility.

4. Conclusion

In this study, IGZO TFTs were developed using siloxane-based SOG as a gate insulator and an interlayer dielectric. The effects of curing the SOG gate insulator in different atmospheres were investigated. The curing of SOG in various atmospheres hardly changed the dielectric properties of the SOG, which played a small role in determining the electrical properties of the TFTs. The surface roughness of the SOG gate insulator was not a major factor in the TFT characteristics, as evidenced by the results of the AFM analysis. The IGZO TFTs with an SOG annealed under an N_2 atmosphere showed the best electrical performance in terms of the on/off drain current ratio, threshold voltage, mobility, and subthreshold slope. This was mainly attributed to the introduction of N_2 at the highest concentration near the interface between the SOG and IGZO active layers, as confirmed by the SIMS analysis.

Disclosure statement

No potential conflict of interest was reported by the authors.

Funding

This work was supported by National Research Foundation: [Grant Number 2017R1D1A1A02019514].

Notes on contributors

Yeong Jo Baek received his B.S. Digital Display Engineering and M.S. Electronic Display Engineering degrees from Hoseo University, Asan, South Korea, in 2017 and 2019, respectively. His current research areas include oxide TFTs, vertical TFTs, interface oxidation, and solution-processed insulators like SOG.

Eui-Jung Yun received his B.S. Electronics Engineering degree from Korea University, Seoul, South Korea, in 1985, and his M.S. and Ph.D. Electrical and Computer Engineering degrees from University of Texas at Austin, Texas, in 1988 and 1994, respectively. From 1994 to 1996, he was a post-doctoral fellow at University of Texas at Austin. In 1996, he joined the faculty of the Department of Electrical, Information, and Communication Engineering of Hoseo University, Chungnam, South Korea. He is currently a professor at the Department of ICT and Automotive Engineering of Hoseo University. His current research areas include the effects of the oxygen ratio on the properties of SnO_2 thin films doped with bismuth, the effects of SF_6 plasma treatment on the properties of IGZO thin films, the effects of post-annealing treatment on the properties of Ga-doped SnO_x thin films, the effects of the structure and sputtering parameters on the device properties of SnO_2 TFTs, and the electrical properties of sputtered SnO-based TFTs.

Byung Seong Bae received his B.S. Atomic Nuclear Engineering degree from Seoul National University, Seoul, South Korea, in 1980, and his M.S. and Ph.D. Applied Physics degrees from Korea Advanced Science and Technology, Seoul, South Korea, in 1986 and 1991, respectively. From 1991 to 1998, he worked at Samsung Electronics, particularly on the development of an amorphous and polysilicon TFT backplane with an integrated driver. From 1999 to 2003, he set up a high-temperature polysilicon TFT microdisplay factory and developed a microdisplay for projection at ILJIN Display. Since 2006, he has been a professor at the

Engineering College of Hoseo University in Asan, South Korea. His current research areas include TFTs, sensors, displays, and integrated circuits of TFTs.

References

[1] M. Da Cheng, T. Luoh, C.T. Su, T.H. Yang, K.C. Chen, and C.Y. Lu, Thin Solid Films **516**, 8726 (2008).

[2] K. Zeng, J.S. Wallace, C. Heimburger, K. Sasaki, A. Kuramata, T. Masui, J.A. Gardella, and U. Singisetti, IEEE Electron Device Lett **38**, 513 (2017).

[3] N.N. Toan, *Ph. D. Thesis, Spin-On Glass Materials and Applications in Advanced IC Technologies,* (International Training Institute for Materials Science (ITIMS), Hanoi, Vietnam, 1999).

[4] C. Avis, Y.G. Kim, and J. Jang, J. Mater. Chem **22**, 17415 (2012).

[5] C. Chiang, D. B. Fraser, Proceedings of Sixth International IEEE VLSI Multilevel Interconnection Conference, Santa Clara, CA, 397, 1989.

[6] M. Dominguez, P. Rosales, A. Torres, M. Moreno, and A. Orduña, Thin Solid Films **520**, 5018 (2012).

[7] M.A. Dominguez, J.A. Luna-Lopez, and S. Ceron, Thin Solid Films **645**, 278 (2018).

[8] J.H. Cheon, J.H. Bae, and J. Jang, IEEE Electron Device Lett **29**, 235 (2008).

[9] M.A. Dominguez, J.L. Pau, and A. Redondo-Cubero, IEEE Trans. Electron Devices **65**, 1014 (2018).

[10] S.H. Hwang, Y.J. Baek, M.T. Hong, S.M. Lee, Y.L. Han, D.S. Moon, E.J. Yun, and B.S. Bae, Jpn. J. Appl. Phys. **57**, 126503 (2018).

[11] M. Dominguez, P. Rosales, A. Torres, F. Flores, J. Molina, M. Moreno, J. Luna, and A. Orduña, Solid. State. Electron. **99**, 45 (2014).

[12] J. Sheng, H.J. Jeong, K.L. Han, T.H. Hong, and J.S. Park, J. Inf. Disp. **18**, 159 (2017).

[13] J.C. Park, S.W. Kim, S. Il Kim, H. Yin, J.H. Hur, S.H. Jeon, S.H. Park, I. Hun Song, Y.S. Park, U.I. Chung, M.K. Ryu, S. Lee, S. Kim, Y. Jeon, D.M. Kim, D.H. Kim, K.W. Kwon, and C.J. Kim, 2009 IEEE International Electron Devices Meeting (IEDM), Baltimore, MD, USA Proceedings, 191, 2009.

[14] M.A. Dominguez, P. Rosales, A. Torres, and M. Moreno, Advanced Materials and Processes for Systems-on-Plastic, Boston, MA, USA Proceedings, K05-01, 2012.

[15] E. Atanassova, G. Tyuliev, A. Paskaleva, D. Spassov, and K. Kostov, Surf. Sci. Spectra **11**, 1 (2006).

[16] Y.S. Lim, Y.J. Im, S.S. Ha, C.H. Park, M.H. Jang, S. Il Choi, J.I. Park, and M. Yi, J. Soc. Inf. Disp. **23**, 384 (2015).

[17] J.-K. Kim, J. Choi, B.S. Bae, and E.-J. Yun, J. Nanosci. Nanotechnol. **17**, 7264 (2017).

[18] P. Barquinha, L. Pereira, G. Gonçalves, D. Kuscer, M. Kosec, A. Vilà, A. Olziersky, J.R. Morante, R. Martins, and E. Fortunato, J. Soc. Inf. Disp. **18**, 762 (2010).

[19] T.T. Korchagina, D.V. Marin, V.A. Volodin, A.A. Popov, and M. Vergnat, Semiconductors **43**, 1514 (2009).

[20] A. Zelenina, A. Sarikov, D.M. Zhigunov, C. Weiss, N. Zakharov, P. Werner, L. López-Conesa, S. Estradé, F. Peiró, S.A. Dyakov, and M. Zacharias, J. Appl. Phys. **115**, 244304 (2014).

[21] R. Salh, *Crystalline Silicon – Properties and Uses* (Intech Europe, Croatia, 2013).

[22] C.E. Viana, A.N.R. da Silva, N.I. Morimoto, and O. Bonnaud, Brazilian J. Phys. **31**, 299 (2001).

[23] P.F. Carcia, R.S. McLean, M.H. Reilly, M.K. Crawford, E.N. Blanchard, A.Z. Kattamis, and S. Wagner, J. Appl. Phys. **102**, 074512 (2007).

[24] R.B.M. Cross, M.M. De Souza, S.C. Deane, and N.D. Young, IEEE Trans. Electron Devices **55**, 1109 (2008).

[25] H. Xie, G. Liu, L. Zhang, Y. Zhou, and C. Dong, Appl. Sci. **7**, 1099 (2017).

[26] C.S. Fuh, S.M. Sze, P.T. Liu, L.F. Teng, and Y.T. Chou, Thin Solid Films **520**, 1489 (2011).

[27] P.T. Liu, C.H. Chang, C.S. Fuh, Y.T. Liao, and S.M. Sze, J. Disp. Technol. **12**, 1070 (2016).

[28] M. Furuta, J. Jianga, G. Tatsuoka, and D. Wang, ECS Trans. **67**, 41 (2015).