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The Effect of Bake Temperature on SU-8 Gate Insulator of IGZO Thin Film Transistor

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SU-8 photoresist was applied to the gate insulator of a-IGZO TFT. The hard bake temperature of SU-8 is important and was varied from 95 to 185 °C. The FTIR showed that hard-bake temperature higher than 125 °C is necessary for complete polymerization. The leakage current and breakdown voltage were improved as increasing hard bake temperatures to 155 °C. However, the crack was generated at 185 °C degrading the electrical characteristics of insulator. The SU-8 insulator was successfully applied to a-IGZO TFT where the on-off ratio was highest for hard-bake temperature of 155 °C.

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I. INTRODUCTION

For high resolution large-size display, active matrix driving with thin film transistor (TFT) is necessary. Hydrogenated amorphous silicon (a-Si:H) TFT is being used widely and low temperature polycrystalline silicon (LTPS) TFT is used for high resolution LCD (liquid crystal display) and organic light emitting diode (OLED) display due to its high mobility and stability [1–3]. Recently, oxide TFTs have received much attention due to their lower cost than LTPS TFT and higher mobility than a-Si:H TFT [4–6]. Most popular material for oxide TFT is amorphous indium gallium zinc oxide (a-IGZO) and a-IGZO TFT is being used for AMOLED TV instead of LTPS TFT.

For high mobility and stability of TFTs, gate insulator and passivation layer as well as active semiconductor layer should be optimized in terms of material and process conditions. Among them gate insulator is first important because the interface states between gate insulator and semiconductor layer is the channel for on current and influence the mobility, threshold voltage and subthreshold slope of TFT.

The conventional gate insulators for TFTs are deposited by vacuum equipment. However, non-vacuum process such as solution process has advantages of printable, low cost and high productivity process [7,8]. Another advantage is non-plasma process which is ion damage free process. In vacuum process high energetic ion of the plasma bombards to the TFT material, which generate defects in the material [9]. In oxide TFT, insulator process is more important than silicon based TFT, because ion bombardment results in high concentration of carrier in IGZO which degrade the TFT characteristics.

The gate insulators by solution process were reported on organic TFT and poly Silicon TFTs using the material such as olefin, parylene, and SU-8 *etc.* [10–12]. SU-8 is stable material used in MEMS and was tested for passivation layers of TFTs including oxide TFT [13–15] but not for gate insulator of the oxide TFT. We applied SU-8 as a gate insulator of the oxide TFT.

SU-8 solution process need bake before exposure and after exposure. Before exposure soft-bake is necessary after spin coating to remove solvent. After soft-bake it is irradiated by UV which initiates cross-linking reaction of epoxy group by the cationic hydrogen H^+ from the photoacid generator (PAG) [15]. The cross-linking reaction is accelerated by thermal energy. For the good

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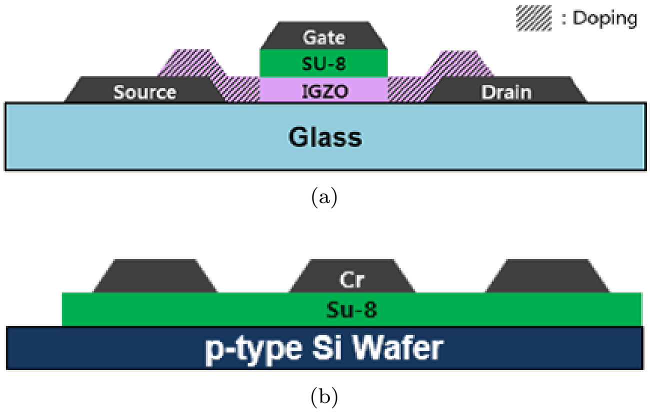

Fig. 1. (Color online) The fabricated oxide TFT with SU-8 gate insulator (a), and MIS capacitor (b).

gate insulator, the hard-bake after exposure is important. The hard-bake temperature and time are key parameters which affects the characteristics of the TFT using gate insulator of SU-8. In this paper, we studied the effect of hard-bake conditions on gate insulator of the IGZO TFT.

II. EXPERIMENTS AND DISCUSSION

Metal-insulator-semiconductor (MIS) structure capacitor and oxide TFT of top gate staggered structure were fabricated with SU-8 insulator as shown in Figs. 1(a) and (b). For source/drain and active layer, about 50 nm thick Cr and IGZO were deposited by sputtering using shadow mask, respectively. After treatment of hexamethyl-disilazane (HMDS) to improve adhesion, SU-8 2000.5 (Microchem) was spin-coated with 2000 rpm for the gate insulator. After spin coating, two step soft-bake was done for 5 min at 65 °C at first and then for 5 min at 95 °C. After soft-bake, it was exposed to 365 nm-13 mJ/s UV for 30 s. After UV exposure, the hard bake was performed under various temperatures with bake time of 20 min to evaluate the effect of hard bake temperature on the gate insulator. The hard bake temperatures were varied from 95 °C to 185 °C. After SU-8 gate insulator, 150 nm thickness Cr was deposited on the SU-8 gate insulator for the gate electrode. For the source and drain region of the oxide TFT, O_2 plasma was treated for 150 s after etching of the gate insulator. For the MIS capacitor, the SU-8 insulator was formed on p-type silicon wafer and the Cr was sputtered on it with shadow mask to form upper electrode as shown in Fig. (b). The diameter of the dot electrode of MIS capacitor was 1 mm and the width and length of the fabricated TFTs were 1000 and 200 μm, respectively.

The thicknesses of the SU-8 insulators with various hard bake temperatures were measured by scanning electron microscope (SEM) and are shown in Table 1.

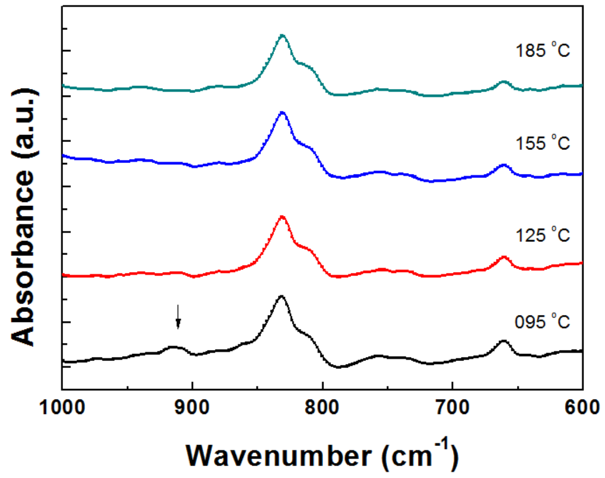

Fig. 2. (Color online) FTIR spectra of SU-8 for various hard-bake temperatures.

Table 1. Thicknesses of SU-8 insulators with various hard-bake temperatures.

Hard-bake temperature [°C]	Thickness [nm]
95	678
125	695
155	736
185	745

Figure 2 shows Fourier transform infrared (FTIR) spectroscopy for SU-8 insulators with various hard bake temperatures to observe the change in the polymerization of SU-8. The peak at 915 cm^{-1} is from epoxy ring due to incomplete polymerization. The peak is observed at hard bake temperature of 95 °C and not observed at the temperatures over 125 °C. That is, SU-8 need the hard bake temperatures higher than 95 °C for the complete polymerization. However, for excessive temperature, crack was observed as shown in Fig. 3.

Figure 3 shows the MIS sample which was composed of top Cr metal/SU-8 insulator/bottom silicon substrate. Because of eight reactive epoxy sites in a monomer of SU-8, the high degree of crosslinking in SU-8 could be achieved after polymerization, which makes the SU-8 insulator stable mechanically and chemically. However, the high young's modulus of 4 to 5 GPa and thermal expansion coefficient of 52 ppm K^{-1} for SU-8 insulator induce large amounts of stress in the insulator layer which creates some cracks in the SU-8 at elevated temperature as shown in Fig. 3.

Dielectric constant K was extracted from the measured capacitance of the MIS sample. Figure 4 shows the dielectric constant (K) for various hard-bake temperatures and frequencies. The electric constant increased as increasing the hard-bake temperatures from 95 °C to 155 °C and the decrease of the dielectric constant was

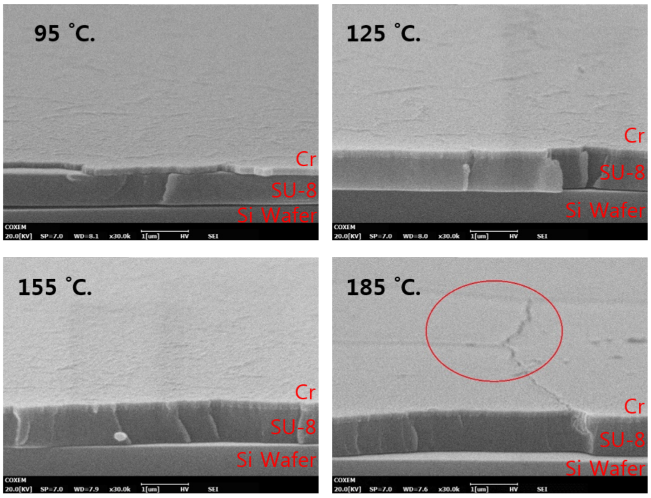

Fig. 3. (Color online) SEM images of SU-8 film for various hard-bake temperatures. The crack on SU-8 was observed at high bake temperature of 185 °C.

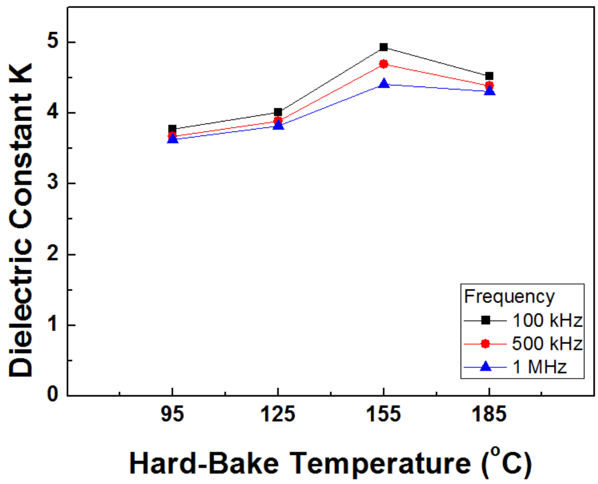

Fig. 4. (Color online) Dielectric constant of SU-8 for various hard-bake temperatures.

Table 2. *C-V* measurements.

Hard-bake Temp. (°C)	Dielectric constant @ 100 kHz	Inflection Voltage (V) @ 100 kHz	Hysteresis (V) @ 100 kHz
95	3.77	26.66	20.98
125	4.01	14.05	8.81
155	4.93	12.31	8.69
185	4.52	10.67	3.89

observed for the hard bake temperature of 185 °C. As shown in Fig. 3, the micro-cracks inside the SU-8 insulators would be easily formed at high bake temperature of 185 °C because the SU-8 insulators have the high thermal expansion coefficient and young's modulus. It is also expected that the micro-cracks in the SU-8 insulators act as a void and their dielectric constants are lower than those of crack-free area in SU-8, resulting in the reduction of the effective dielectric constant of the SU-8 insulators. As a result, the reduced capacitance at bake temperature of 185 °C was associated with the micro-cracks inside the SU-8 film. Therefore, the decrease of the dielectric constant at the bake temperature of 185 °C was attributed to the cracks inside the SU-8 insulator.

The capacitance-voltage (*C-V*) measurement result of MIS sample is shown in Table 2 which shows the inflection voltage and hysteresis of the SU-8 insulators with various hard bake temperatures. The inflection voltage extracted from *C-V* measurement corresponds to flat band voltage which is defined as the voltage required to achieve the flat band condition [16]. The accumulated charges in the insulator and at the semiconductor-oxide interface result in the band bending near the semiconductor surface, which in turn induces the changes of the flat band voltage. The positive flat band voltage is originated from the negative charges trapped at defects inside the gate insulator or near the IGZO semiconductor-SU-8 insulator interface. Therefore, the decrease in the flat band voltages at a higher bake temperature suggests that the number of trapped charges decreases due to the reduction of defect densities inside the gate insulator or near the semiconductor-insulator interface. The decrease in the number of trapped charges can reduce the hysteresis characteristics for TFTs, resulting in the improvement of the stability of TFTs. Since the hysteresis is the change of flat band voltage, the hysteresis was usually obtained from inflection voltage changes during *C-V* measurements. Therefore, the decreased hysteresis is consistent with the reduced inflection voltages in terms of decreased defect states.

Figure 5 shows the current-voltage characteristics of SU-8 insulators treated with various hard bake temperatures, indicating that the leakage current and dielectric strength of SU-8 insulators were improved with increasing polymerization by the increase in the hard bake temperature. The SU-8 films baked at 95 °C exhibited a high leakage current at low electric field region of 0 - 0.5 MV/cm. For SU-8 films treated with the bake temperature of 95 °C, the FTIR results shown in Fig. 2 reveals the peak at 915 cm^{-1} which is attributed to the epoxy ring due to incomplete polymerization. The incomplete polymerization and remaining solvent can increase the leakage current caused by ions in the material. It was known [17] that the removal of the solvent is important in organic SU-8 insulator and the solvent should be eliminated completely to achieve the low leakage current. As increasing the bake temperature, the FTIR peak from epoxy ring due to incomplete polymerization weakens and disappears as shown in Fig. 2. We can conclude from the results in Figs. 2 and 5 that the leakage current and breakdown voltages of SU-8 films are improved with increasing the polymerization by the increased bake

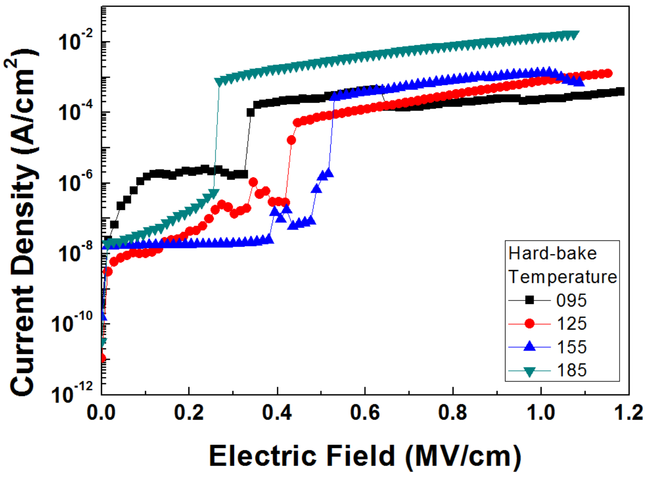

Fig. 5. (Color online) Current-voltage characteristics of SU-8 insulators with various hard-bake temperatures.

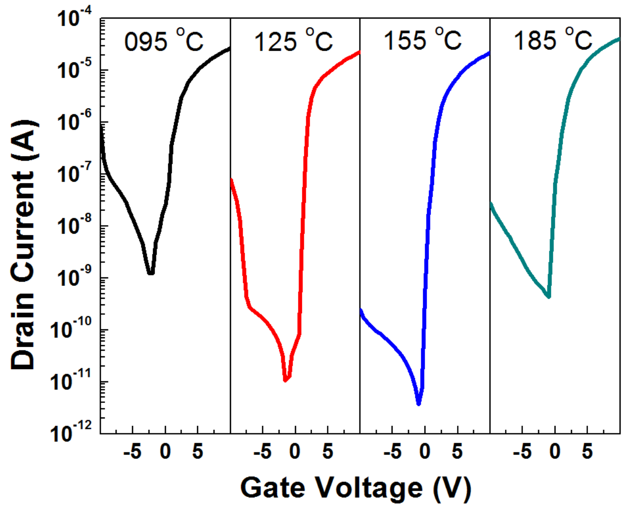

Fig. 6. (Color online) Transfer curves of developed oxide TFTs with various hard bake temperatures of SU-8 insulators. Drain-source voltage was 10 V.

temperatures. Therefore, the complete polymerization is important for device applications in terms of low leakage current and high breakdown voltage. However, for the case of bake temperature of 185 °C, the leakage current of SU-8 films increased once again. This increase in the leakage current at the bake temperature of 185 °C was attributed to the cracks inside the SU-8 insulator, as evident in Fig. 3.

For hard bake temperature of 155 °C, breakdown electric field was 0.4 MV/cm. However, when the hard-bake temperature was increased to 185 °C, breakdown voltage decreased again, which was attributed to the generated crack inside the insulator as shown in Fig. 3. Generated crack results in increase of leakage current and decrease of the breakdown voltage.

The transfer characteristics of the IGZO TFT with SU-8 gate insulators are shown in Fig. 6 for various hard bake temperatures. As increasing hard-bake temperatures from 95 °C to 155 °C, gate leakage current was decreased effectively. The higher hard-bake temperature reduces the defect density by the stronger polymerization as shown in Fig. 2 and Table 2, which reduces the leakage current and increased the on/off ratio of the IGZO TFTs. The leakage current increased again when the hard-bake temperature was 185 °C due to the crack inside the insulator as shown in Fig. 3.

III. CONCLUSION

Solution based gate insulator SU-8 was applied to the IGZO TFT and optimized the hard bake condition. The MIS device was fabricated to evaluate the insulator and current-voltage characteristics and capacitance voltage characteristics were performed with the MIS device. The effect of hard bake temperatures of SU-8 on the insulator was evaluated.

The FTIR spectra showed that hard-bake temperature higher than 125 °C is necessary for complete polymerization. The leakage current and breakdown voltage were improved as increasing hard bake temperatures from 95 °C to 155 °C. However, the crack was generated at 185 °C which degraded the electrical characteristics of insulator. The SU-8 insulator was applied to a gate insulator of the top gate IGZO TFT. The leakage current was lowest for the SU-8 gate insulator with the hard-bake temperature of 155 °C. For the higher bake temperature of 185 °C the on-off ratio of the a-IGZO TFT decreased due to the crack inside the insulator.

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