BCD to 7-segment decoder with oxide thin film transistors

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Binary coded decimal (BCD) to 7-segment decoder with oxide thin film transistors (TFTs) was implemented on a glass to display 7-segment display from BCD. The developed BCD to the 7-segment decoder with indium–gallium–zinc oxide thin film transistors was verified up to 1 kHz operation frequency under the power supply voltage of 5 V, and converted successfully 4-bit binary input code to 7-segment inputs. The binary output voltages were 0.4 V for the low and 4.1 V for the high at an operation frequency of 500 Hz, respectively. The output signals of the developed 7-segment decoder matched well the BCD to the decimal values. The result showed that oxide TFT can be used for the integrated BCD to 7-segment decoder for the various sensing applications, particularly for wearable devices and the integrated bio sensing platform.

Introduction: Oxide semiconductor thin film transistors (TFTs), such as amorphous indium–gallium–zinc oxide (a-IGZO) TFTs, are replacing the amorphous silicon (a-Si:H) TFTs owing to higher mobility and better uniformity than a-Si:H TFT as well as process compatibility with the a-Si:H TFT as the resolution and size of the display increase [1, 2]. Owing to transparency and higher mobility than amorphous silicon TFTs, a-IGZO TFTs have been studied widely and various integrated circuits, such as the pixel circuit, scan drivers, inverter, ring oscillator and logic gates have been reported [3–8].

Since p-channel operation is difficult due to the large density of states below the Fermi level, a-IGZO TFT circuits should be developed with only n-channel TFTs, and a few papers have been published on logic gates. The a-IGZO TFT logic gates, such as NAND and NOR, were reported with an operation frequency of 5 kHz at $V_{DD} = 10$ V [9]. And also, the ROM driver for RFID was reported with IGZO TFTs [8]. However, thus far, there was no report on BCD (binary coded decimal) to 7-segment decoder which is necessary for displaying sensing signal in an embedded circuit such as an integrated bio sensing platform.

The oxide TFT was fabricated using a methyl-siloxane based organic spin on glass (SOG) passivation layer, which reduces the plasma damage on the active layer [10]. After examining the bootstrapped inverter and NAND gates with a-IGZO TFTs, a BCD to 7-segment decoder, which can be integrated on a substrate to drive a 7-segment display, was developed. The 7-segment decoder circuit is useful for displaying sensing signal in integrated circuits such as fully integrated bio sensing platforms, which include a 7-segment display as well as sensors, amplifiers, data processors and so on.

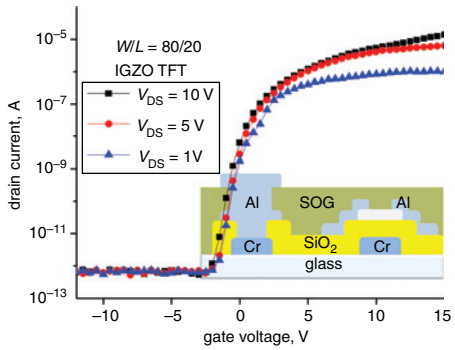

Fig. 1 *Transfer characteristics of IGZO TFT and the inset is cross-sectional structure of fabricated TFT*

Experimental: The bottom-gate IGZO TFTs were fabricated with SOG passivation. A 150-nm-thick Cr layer was deposited at room temperature by sputtering and patterned for a gate electrode by wet etching. A 300-nm-thick SiO_2 was deposited as a gate insulator by plasma-enhanced chemical vapour deposition, and a 50-nm-thick a-IGZO layer was then deposited at 250°C by sputtering as a channel material and patterned by wet etching. A 110-nm-thick Al layer was deposited for the source/drain electrodes. After patterning the source/drain electrodes, a 320-nm-thick methyl-siloxane based organic passivation layer was spin coated followed by annealing at 350°C. Finally, a 110-nm-thick Al layer was formed for the electrodes after contact hole etching on the SOG passivation layer. Fig. 1 shows the transfer characteristics of the fabricated IGZO TFT. At $V_{DS} = 5$ V, the device exhibited a field effect mobility of 2.88 cm^2/Vs, a threshold voltage of 0.37 V, and a subthreshold slope of 0.40 V/dec.

Fig. 2*a* shows the bootstrapped inverter using a diode connected TFT (T1), a load TFT (T2) with $W/L = 10/10$ and a drive TFT (T3) with $W/L = 80/10$. The full V_{DD} output high voltage can be obtained through the use of bootstrapped inverters. Boot-strapping is a technique by which the gate voltage of the load transistor (T2) is driven to a bias higher than V_{DD} by the positive feedback through capacitor C1 and the parasitic capacitance of T2 during the output high transient. Fig. 2*b* shows the developed NAND gate.

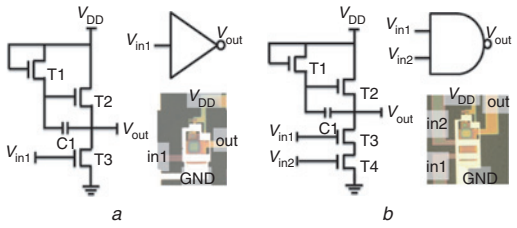

Fig. 2 *Circuits and micrographs for*
a Inverter and
b NAND gate

The 7-segment decoder circuit was designed and fabricated (7.0 × 5.2 mm) with a-IGZO TFTs on a glass substrate, as shown in Fig. 3*a*. The input and output waveforms are shown in Fig. 3*b*. The outputs (a–g) of the 7-segment decoder were evaluated with four input signals (A, B, C, and D). At step 1, as shown in Fig. 3*a*, the outputs (P0–P9) are generated according to the four inputs of A, B, C, and D. At step 2, the output signals (a–g) for displaying the 7-segment display are generated by NAND gates connected to the outputs P0–P9. Each output signal of a–g corresponds to each input of the 7-segment display. Output signals of a–g turn on the required segments of the 7-segment display for the decimal number corresponding to the input BCD.

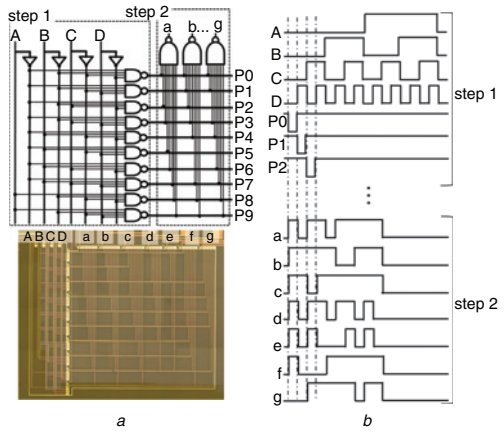

Fig. 3 *The fabricated circuit and timing chart of the signals*
a BCD to 7-segment decoder circuit and optical micrograph of fabricated circuit
b Input and output waveforms of circuit

Results and discussion: Fig. 4*a* shows the input and output waveforms of the inverter with a supply voltage of $V_{DD} = 5$ V. The top is the input clock and the second, third and fourth are the outputs for 62.5, 250 and 1 kHz input clocks, respectively. Fig. 4*b* shows two inputs and output waveforms of the NAND gate. The first and second are two inputs and the bellows are the outputs for various input frequencies of 62.5, 250 Hz and 1 kHz. The output voltages of the inverter and NAND gate were 4.8 V for the high and 0.2 V for the low. The rise and fall times of the inverter were 500 and 60 µs, respectively, and 500 and 90 µs for the NAND gate.

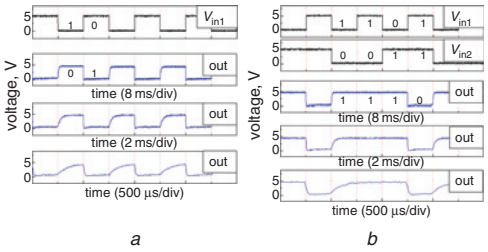

Fig. 4 *Input and output waveforms of*

a Inverter and

b NAND gate, operated at 62.5, 250 Hz and 1 kHz with supply voltage of V_{DD} = 5 V

Even the rise and fall times are rather long due to the low operation voltage of V_{DD} = 5 V, the circuit is compatible with 5 V logic and suitable for low speed applications.

Fig. 5 shows the four BCD inputs and output waveforms of the 7-segment decoder. The input frequency of BCD was a 500 Hz and a voltage swing was 0–5 V. Among the four BCD inputs, 'D' is the least significant bit and 'A' is the most significant bit, and the inputs were generated in sequence to represent 0–9. The outputs are labelled as a, b, c, d, e, f, and g which correspond to each segment of 7-segment display. The logic '1' corresponds to the light-on of segment. Therefore, four input bits A, B, C, and D specify numbers from 0 to 9, and the seven output bits (a, b, c, d, e, f, g) specify which segment should light on in a 7-segment. The output voltage swing was from 0.4 to 4.1 V, and the rise and fall times under the oscilloscope input capacitance were 650 and 150 µs, respectively. The 7-segment display corresponding to the outputs are depicted at the lowest shown in Fig. 5.

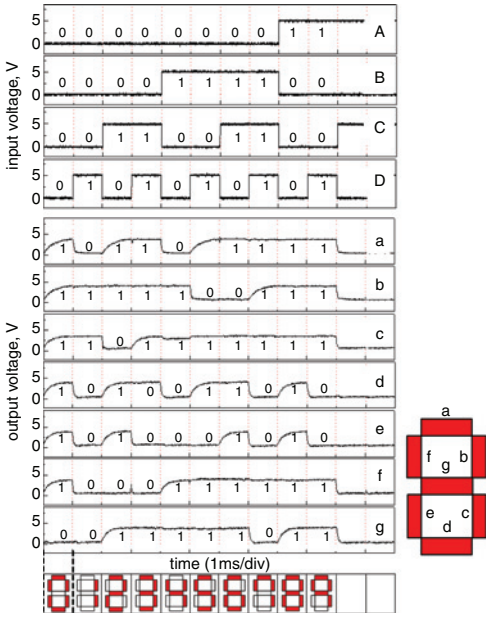

Fig. 5 *Measurement result of 7-segments decoder operated at 500 Hz under power supply voltage of V_{DD} = 5 V*

These results verify that the developed 7-segment decoder converts well the input BCD to 7-segment display inputs for the display of corresponding decimal.

Conclusion: Based on a-IGZO TFTs, the BCD to 7-segment decoder was developed. Bootstrapped inverters and NAND gates were adopted to overcome the decreased swing of output voltage caused by the use of only *n*-type a-IGZO TFTs. The operations of the inverter and NAND gate were verified up to a 1 kHz frequency under the power supply voltage of V_{DD} = 5 V. The developed BCD to 7-segment display decoder showed that the swing of the output voltages were from 0.4 to 4.1 V at an operation frequency of 500 Hz under the power supply voltage of V_{DD} = 5 V, and the input 4 bit binary codes were converted successfully to a 7-segment display input signal. The developed BCD to 7-segment decoder is much useful for the various applications, such as wearable devices and fully integrated bio sensing platforms which include display on them.

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One or more of the Figures in this Letter are available in colour online.

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References

1 Neg, M., Muller, R., Steudel, S., *et al.*: 'Low-temperature formation of source-drain contacts in self-aligned amorphous oxide thin-film transistors', *J. Inf. Displ.*, 2015, **16**, (2), pp. 111–117
2 Kang, J.-S., and Kwon, O.-K.: 'Low-power and small-area scan driver using depletion-mode a-IGZO TFTs for ultra-high-resolution display', *Electron. Lett.*, 2012, **48**, (20), pp. 1268–1269
3 Lee, J.P., Hwang, J.Y., and Bae, B.S.: 'Pixel circuit with threshold voltage compensation using a-IGZO TFT for AMOLED', *J. Semicond. Tech. Sci.*, 2014, **35**, (1), pp. 72–74
4 Lee, J.W., Kim, S.Y., Kim, S.O., *et al.*: 'A scan driver circuit for depletion-mode oxide TFTs with stable output waveforms', *J. Inf. Displ.*, 2014, **15**, (4), pp. 207–212
5 Kim, B., Ryoo, C.I., Kim, S.J., *et al.*: 'New depletion-mode IGZO TFT shift register', *Electron Device Lett.*, 2011, **32**, (2), pp. 158–160
6 Suresh, A., Wellenius, P., Baliga, V., *et al.*: 'Fast all-transparent integrated circuits based on indium gallium zinc oxide thin-film transistors', *Electron Device Lett.*, 2010, **31**, (4), pp. 317–319
7 Nam, H., and Song, E.J.: 'Oxide TFT inverter with wide output dynamic range', *Electron. Lett.*, 2012, **48**, (13), pp. 791–792
8 Yang, B.-D., Oh, J.-M., Kang, H.-J., *et al.*: 'A transparent logic circuit for RFID Tag in a-IGZO TFT technology', *ETRI J.*, 2013, **35**, (4), pp. 610–616
9 Luo, H., Wellenius, P., Lunardi, L., and Muth, J.F.: 'Transparent IGZO-based logic gates', *Electron Device Lett.*, 2012, **33**, (5), pp. 673–675
10 Bermundo, J.P., Ishikawa, Y., Yamazaki, H., Nonaka, T., and Uraoka, Y.: 'Highly reliable polysilsesquioxane passivation layer for a-InGaZnO thin-film transistors', *ECS J. Solid State Sci. Technol.*, 2013, **3**, (2), pp. 16–19