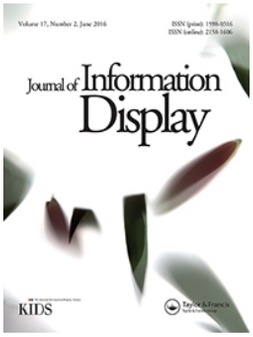

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Analog-to-digital converter with oxide thin-film transistors

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ABSTRACT

A three-bit flash analog-to-digital converter (ADC) consisting of inverter-based comparators and logic gates using amorphous indium-gallium-zinc-oxide thin-film transistors (a-IGZO TFTs) was developed. The TFT has a bottom gate structure with a methyl-siloxane-based organic spin-on-glass passivation layer, which reduces the plasma damage on the active layer. A bootstrapped logic gate structure was used in the proposed ADC to overcome the reduced output swing in the inverters and the NAND gates caused by using only n-type a-IGZO TFTs. The output signals of the developed three-bit flash ADC with a-IGZO TFTs well matched the analog inputs. The output voltage swing was 0.2–3.6 V, well matching the simulation result. The three-bit flash ADC was verified up to the 1 kHz operation frequency, and thus can be used in sensor applications such as the wearable sensor display and the integrated biosensing platform.

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KEYWORDS
three-bit flash AD converter; logic gates; oxide thin-film transistor

Introduction

Oxide semiconductor thin-film transistors (TFTs) such as amorphous indium-gallium-zinc-oxide (a-IGZO) TFTs show better performance than amorphous silicon TFTs and are increasingly becoming widely used for the display backplane as the resolution and size of the display increases [1–4]. Owing to their transparency and higher mobility compared to the amorphous silicon TFTs, a-IGZO TFTs have been studied widely, and various integrated circuits, such as the pixel circuit, scan drivers, inverter, ring oscillator, and logic gates, have been reported [5–14]. As p-channel operation is difficult due to the large density of states below the Fermi level, a-IGZO TFT circuits have been implemented with only n-channel TFTs.

Reported in this paper is the design of a three-bit flash analog-to-digital converter (ADC) using oxide TFTs that can be used in the integrated biosensor platform. The integrated biosensor platform requires ADC for analog-to-digital conversion for the processing of the data. The analog-to-digital conversion is an inherently slow process, and the speed of the conversion depends on the conversion scheme consisting of a variety of circuit blocks.

Flash ADC is one of the commonly used converters for bit numbers less than or equal to 8, and it has the fastest conversion speed among all the types of ADC circuits [15]. Few papers on flash ADCs using TFTs such as a-Si:H and polysilicon TFT, however, have been reported with five- and three-bit ADCs [16–18].

The developed ADC consists of an inverter-based comparator and an encoder with n-channel a-IGZO TFTs. The TFTs have a bottom gate structure with a methyl-siloxane-based organic spin-on-glass (SOG) passivation layer, which reduces the plasma damage on the active layer [19]. After examining comparators and logic gates with a-IGZO TFTs, a three-bit ADC was developed. The three-bit flash ADC is useful for the integrated sensing platform, in which it converts the sensing signal to a digital signal.

Experiment

The bottom-gate IGZO TFTs were fabricated with an SOG passivation layer, as shown in Figure 1. A 150-nm-thick Cr layer was deposited at room temperature by sputtering, and was patterned for a gate electrode through wet etching. A 300-nm-thick SiO_2 layer was deposited as a gate insulator through plasma-enhanced chemical vapor deposition, and a 50-nm-thick a-IGZO layer was then deposited at 250°C through sputtering as a channel material, and was then patterned through wet etching. As the IGZO layer is etched out during the source drain wet

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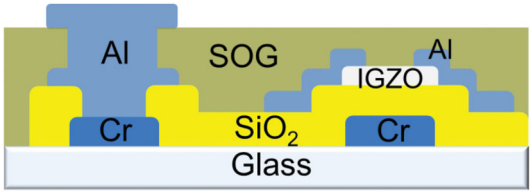


Figure 1. Cross-sectional structure of the fabricated TFT.

etching, the metal etchant was diluted to reduce the etch rate of the IGZO, and the overetch time was controlled. After the source/drain electrode patterning through wet etching, a 320-nm-thick methyl-siloxane-based organic passivation layer was spin-coated, followed by annealing at 350°C. Finally, a 110-nm-thick Al layer was formed for the electrodes after contact hole etching on the SOG passivation layer.

The logic circuits in the encoder for ADC were implemented using the bootstrapped concept. The basic logic gates were developed with IGZO TFTs. Figure 2(a) shows the bootstrapped inverter using a diode-connected TFT (T1), a load TFT (T2) with $W/L = 10/10$, and a drive TFT (T3) with $W/L = 80/10$. The full V_{DD} output high voltage can be obtained using bootstrapped inverters [20]. Bootstrapping is a technique by which the gate voltage of the load transistor (T2) is driven to a bias higher than V_{DD} by the positive feedback through capacitor C1 and the parasitic capacitance of T2 during the output high transient. Figure 2(b) shows the developed NAND gate.

Shown in Figure 3 is a three-bit flash ADC schematic, a three-bit A/D converter consisting of seven comparators and an encoder. The comparators include a bootstrapped inverter consisting of two input switching TFTs (T1, T3), one connected TFT (T2), and two coupling capacitors (C1, C2). T1 is used to introduce the reference voltage to node A, T2 is used to connect the input and output of the inverter to set the initial state of the inverter of the comparator, and T3 is used to introduce the input analog voltage to node A. The reference voltages for the compactors are generated by a serially connected resistor array of eight 1 kΩ resistors. These reference voltages are compared to the analog input voltage by the comparators, which output "0" or "1" according to the analog input voltage. Then the binary outputs of the comparator are converted to the binary format (A2, A1, A0) by a digital encoder during CLK 4 high.

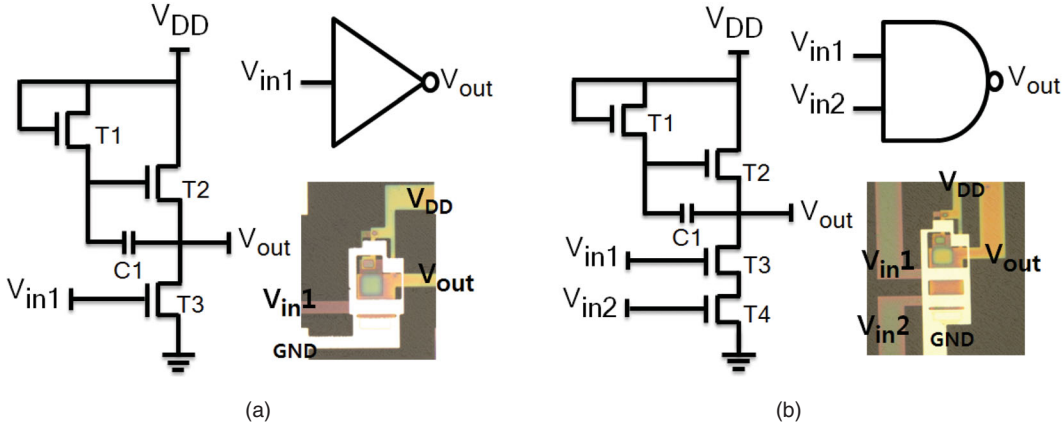


Figure 2. Logic circuit and optical micrographs of the (a) inverter and (b) NAND gate.

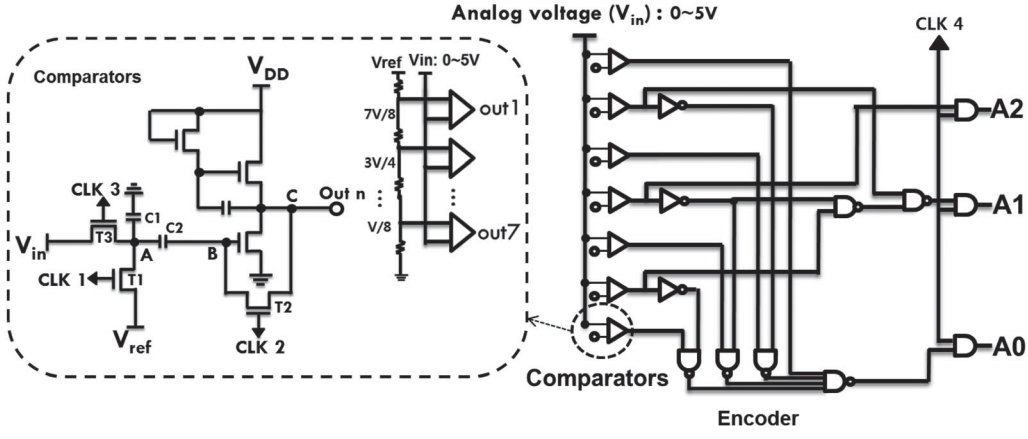


Figure 3. Three-bit flash ADC schematic.

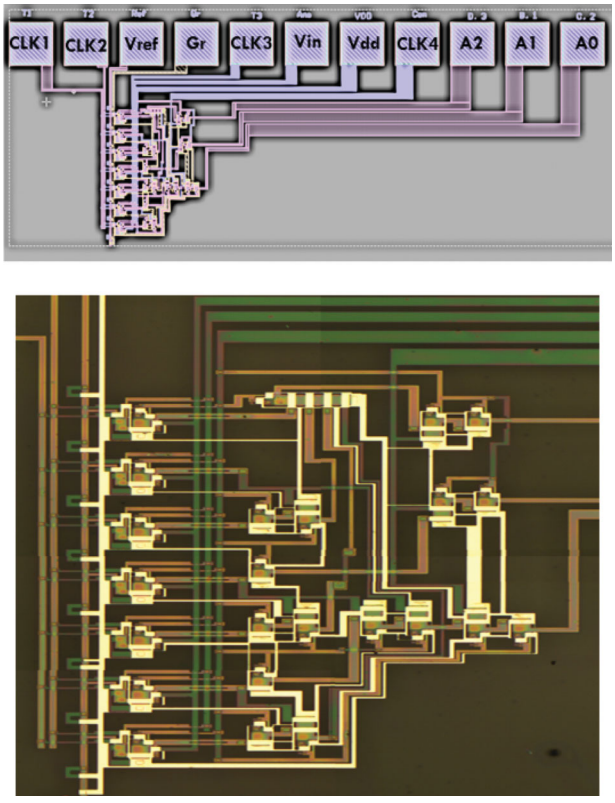


Figure 4. Layout design and optical micrographs of the three-bit flash ADC.

Based on the above configuration, a three-bit flash ADC was designed and implemented with a-IGZO TFTs. The design layout and the optical micrograph of the fabricated three-bit flash ADC with a-IGZO TFTs are shown in Figure 4. The fabricated ADC has 11 interface metal pads for four input CLKs, one analog input, one reference input, one V_{DD}, and three outputs. The ADC design occupies an about $2 \times 3\ mm^2$ effective area.

Results and discussion

Figure 5 shows the transfer characteristics of the fabricated a-IGZO TFT. At $V_{DS} = 5\ V$, the device exhibited $2.88\ cm^2/Vs$ field effect mobility, a 0.37 V threshold voltage, and a 0.40 V/dec subthreshold slope.

The output signal was monitored while varying the input voltages from 0 to 5 V with the power voltage of $V_{DD} = 5\ V$. Figure 6(a) shows the input and output waveforms of the inverter under $V_{DD} = 5\ V$. The first one from the top is the input, and the second, third, and fourth are the outputs for the 62.5 Hz, 250 Hz, and 1 kHz input frequencies, respectively. Figure 6(b) shows the input and output waveforms of the NAND gate. The first and second from the top are the two inputs to the NAND, and the others are the outputs for various input frequencies (62.5 Hz, 250 Hz, and 1 kHz). The output voltages of the inverter and NAND gate were 4.8 V for the high state

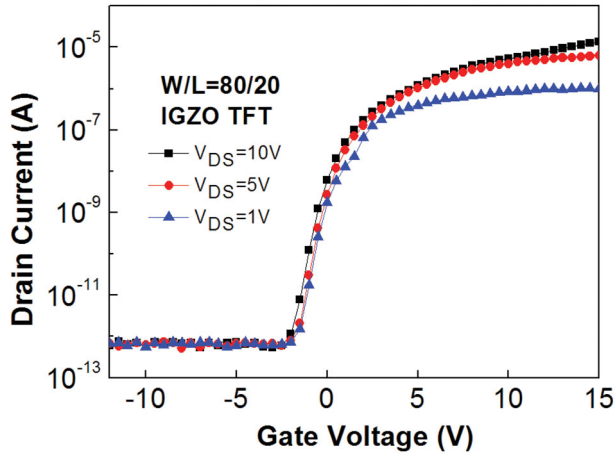


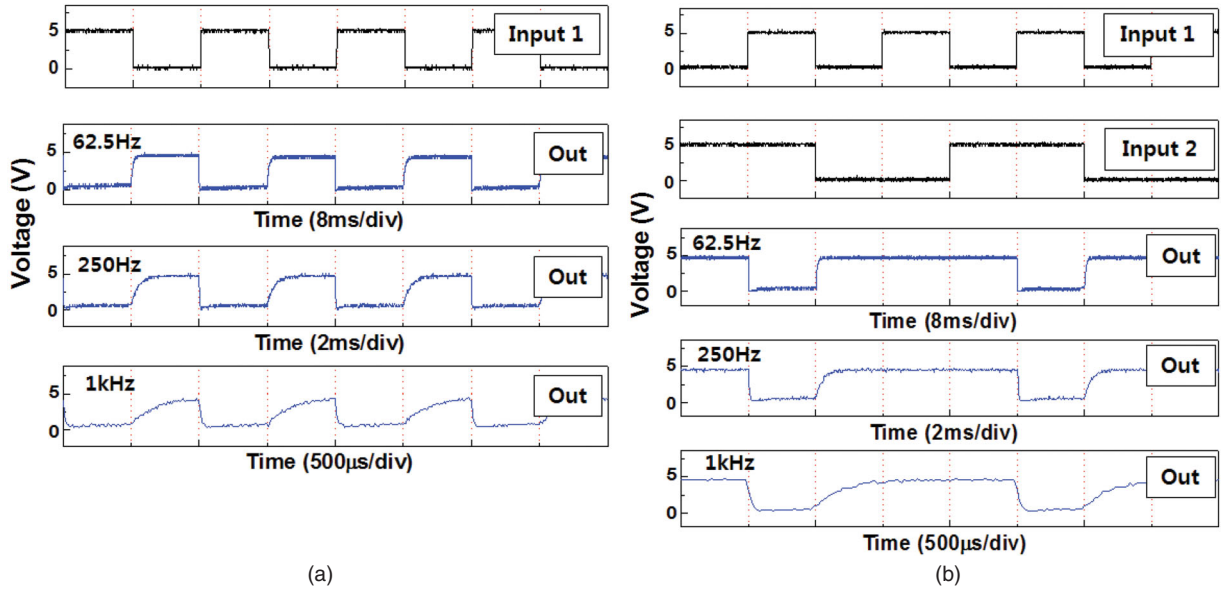
Figure 5. Transfer characteristics of the fabricated IGZO TFT.

and 0.2 V for the low state. These outputs were labeled "0" and "1". The rise and fall times of the inverter were 500 and 60 μs, respectively, and 500 and 90 μs for the NAND gate. Although the rise and fall times were rather long due to the low operation voltage of $V_{DD} = 5\ V$, the circuit is compatible with the 5 V logic and is suitable for low-speed applications.

The operation of the inverter-based ADC comparator is illustrated in the simulation results shown in Figure 7(a) and 7(b). When CLK 1 is high, the reference voltage is introduced to node A of the comparator. When TFT T2 is turned on by CLK 2, the voltages of nodes B and C become the same through the connection of the said nodes.

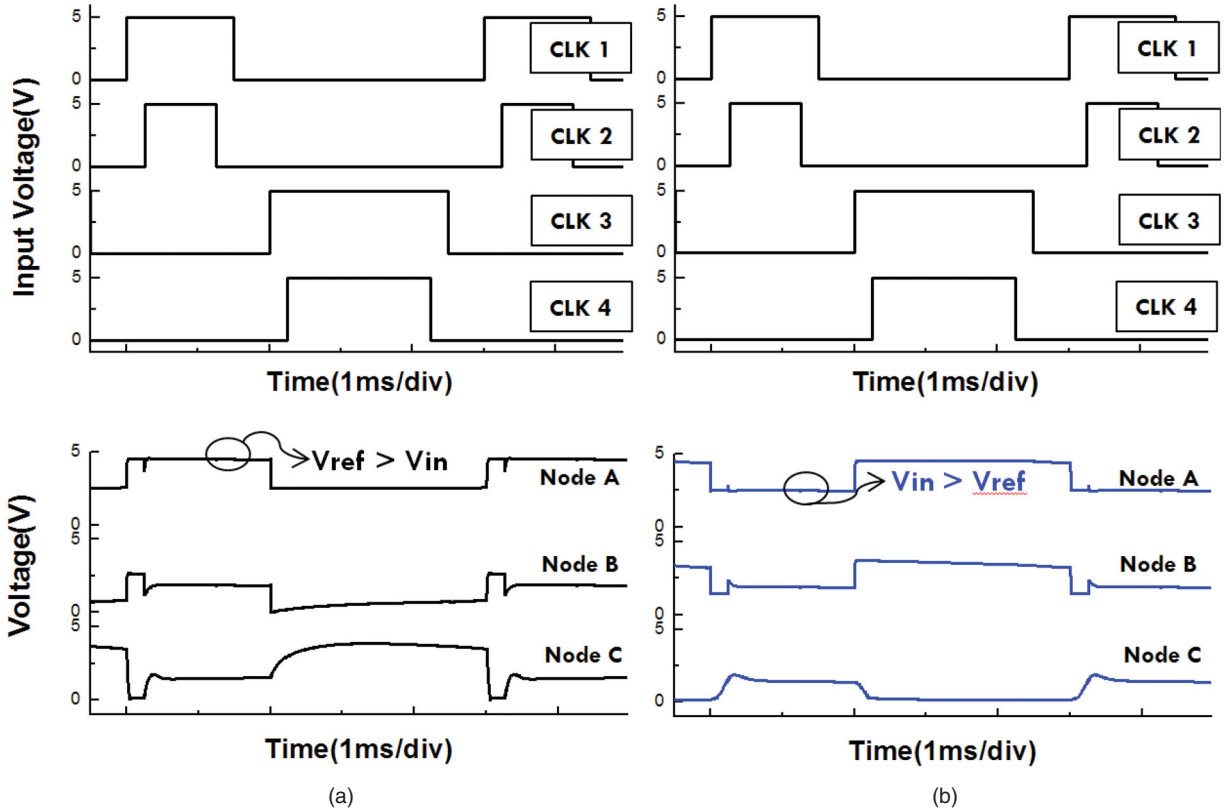
Then, while CLK 3 turns on T3, the analog input voltage (V_{in}) is introduced to node A of the comparator. At this time, the voltage of node A decreases (Figure 7(a)) when the analog input voltage is lower than the reference voltage, and increases (Figure 7(b)) when the input voltage is higher than the reference voltage. According to the increase or decrease of the voltage at node A, the voltage at node B also increases (Figure 7(a)) or decreases (Figure 7(b)) owing to coupling capacitor C2. Therefore, the voltage at node C, which is the output of the inverter, becomes high (Figure 7(a)) or low (Figure 7(b)) according to the comparison result of the input voltages to the reference voltage. Therefore, the output of the comparator becomes low when the input voltage is higher than the reference voltage, and becomes high when the input voltage is lower than the reference voltage.

The input analog voltage is compared to the reference voltages generated by the serially connected resistor array. Then a three-bit code (A2, A1, A0) corresponding to the input analog voltage is generated from the outputs of the comparators. The comparator outputs are encoded to the three-bit code by the encoding circuit during CLK 4 high, as shown in Figure 8.



(a) (b)

Figure 6. Input and output waveforms of the (a) inverter and (b) NAND gate operated at 62.5 Hz, 250 Hz, and 1 kHz with a $V_{DD} = 5$ V supply voltage.



(a) (b)

Figure 7. CLK inputs of the ADC and operating simulation results of the comparator. (a) $V_{ref} > V_{in}$; (b) $V_{in} > V_{ref}$.

Figure 8 shows the simulation results of the three-bit ADC for various analog inputs. Figure 8 shows the waveforms of the three-bit binary-code outputs (A2, A1, A0) with a 5 V power supply at a 500 Hz operation frequency with a clock voltage of 5 V. The voltage of one least significant bit (LSB) is 0.625 V with three bits, and the analog input voltages from 0 to 5 V are correctly converted to three-bit binary codes (111–000).

Figure 9(a) and 9(b) shows the measurement results for the fabricated three-bit ADC. The four input CLKs and all the three output signals are presented for the operating frequencies of 500 Hz (Figure 9(a)) and 1 kHz

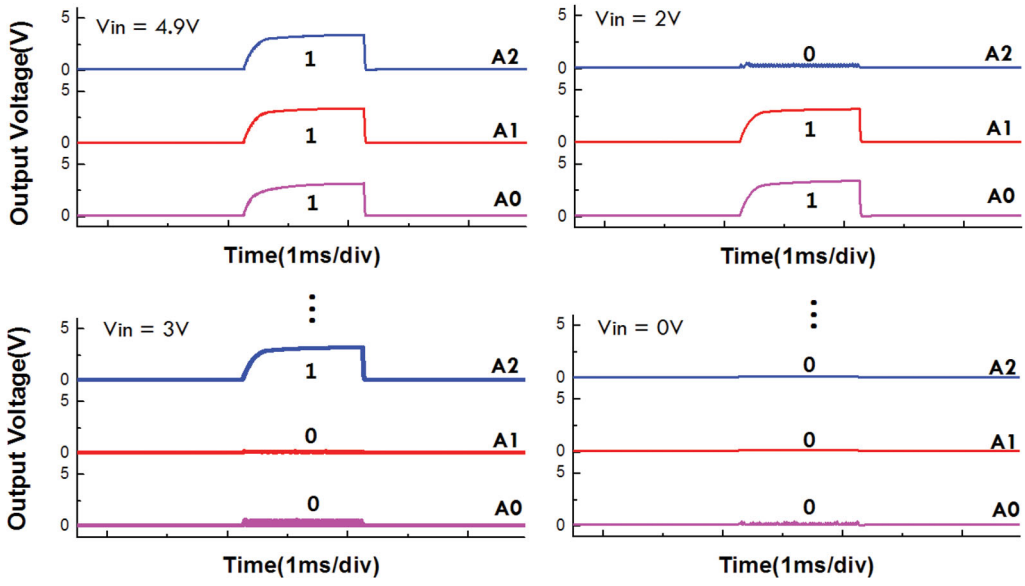


Figure 8. Simulation results of the ADC at a $V_{DD} = 5$ V supply voltage and operating at 500 Hz.

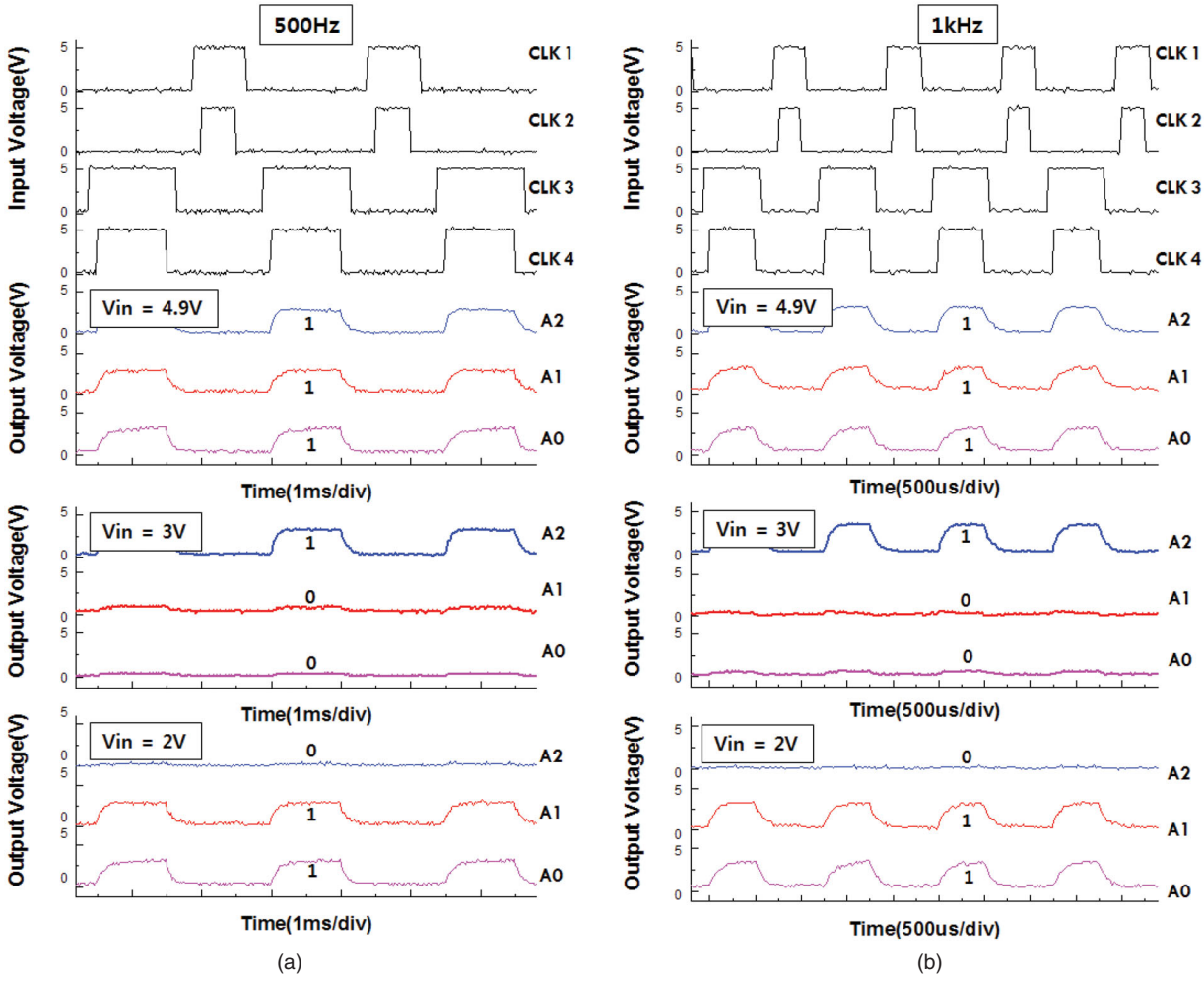


Figure 9. Measurement results of the ADC at a $V_{DD} = 5$ V supply voltage and with 4.9, 3, and 2 V analog voltage changes, operating at (a) 500 Hz and (b) 1 kHz.

(Figure 9(b)). Among the three output bits, "A0" is the least significant bit, and "A2" is the most significant bit. Each analog voltage was converted to the binary code, as shown in Figure 9(a) and 9(b), such as 4.9 V to 111, 3 V to 100, and 2 V to 011. The output voltages were 0.2 V for the low state and 3.6 V for the high state. The developed three-bit flash ADC with oxide TFTs successfully converts the analog input voltage to the three-bit binary code and can be useful for the integrated TFT sensor platform, particularly for converting the sensing signal to a digital signal.

Conclusions

Based on a-IGZO TFTs, a three-bit flash ADC was developed with a combination of an inverter-based comparator and logic gates. Bootstrapped logic gates and comparators were applied to overcome the narrow swing output voltage caused by the use of only n-type a-IGZO TFTs. The operation of the logic gates was verified up to a 1 kHz frequency under the operation voltage of $V_{DD} = 5$ V.

At 1 LSB 0.625 V, the simulation results of the three-bit ADC on various analog inputs, the waveforms of three-bit binary-code outputs with a 5 V power supply at a 500 Hz operation frequency with a 5 V clock voltage, were converted to three-bit binary codes (111–000) according to the analog input voltages (0–5 V).

As with the simulation results, the measurement results of the developed three-bit flash ADC showed that the swings of the output voltages were 0.2 and 3.6 V at a 1 kHz operation frequency under a $V_{DD} = 5$ V operation voltage. The output signals of the developed three-bit flash ADC with a-IGZO TFTs matched the three-bit digital code to the analog input changes (e.g. 4.9 V to 111, 3 V to 100, and 2 V to 011).

For the sensor system, the developed ADC can be used to convert the sensing signals at the sensor node, and to transport the digital signals to the external interface. Also, oxide TFTs can be used for the integrated ADC for various sensing applications, such as the fully integrated biosensing platform, which is transparent and flexible.

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Jun Young Hwang received his BS Digital Display Engineering degree from Hoseo University, Asan, South Korea in 2014, and is currently working toward an MS Display Engineering degree from the same university. His research interests include lenticular-lens LC, oxide pixel circuit design for AMOLED applications, and oxide-TFT-based integrated circuit design for the fingerprint sensor and biosensing display platform.

Min Taek Hong received his first BS degree (BS Defense Science Technology) and his second BS degree (BS Optoelectronic Display Engineering) from Hoseo University in 2010 and 2016, respectively. After graduation, he joined the Electronic Device Laboratory of the Display Engineering Department of Hoseo University in 2016. His research area is the sputtered-SiO_2 and solution-processed SOG gate insulator.

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Byung Seong Bae received his BS Atomic Nuclear Engineering degree from Seoul National University, Seoul, South Korea in 1984, and his MS and PhD Applied Physics degrees from the Korea Advanced Institute of Science and Technology, Seoul, South Korea, in 1986 and 1991, respectively. Between 1991 and 1998, he worked at Samsung Electronics, particularly on the development of amorphous and polysilicon TFT LCDs with an integrated driver. From 1999 to 2003, he set up a high-temperature polysilicon TFT LCD factory and developed a microdisplay for projection displays at ILJIN Display. Since 2006, he has been a professor at the Engineering College of Hoseo University in Asan, South Korea.

References

[1] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano and H. Hosono, Nature **432** (7016), 488 (2004).
[2] A. Sato, M. Shimada, K. Abe, R. Hayashi, H. Kumomi, K. Nomura, T. Kamiya, M. Hirano and H. Hosono, Thin Solid Films **518** (4), 1309 (2009).
[3] M. Nag, R. Muller, S. Steudel, S. Smout, A. Bhoolokam, K. Myny, S. Schols, J. Genoe, B. Cobb, A. Kumar, G. Gelinck, Y. Fukui, G. Groeseneken and P. Heremans, J. Inf. Disp. **16** (2), 111 (2015).
[4] J.Y. Kwon, K.S. Son, J.S. Jung, T.S. Kim, M.K. Ryu, K.B. Park, B.W. Yoo, J.W. Kim, Y.G. Lee, K.C. Park, S.Y. Lee and J.M. Kim, IEEE Electron Dev. Lett. **29** (12), 1309 (2008).
[5] K.H. Lee, J.S. Jung, K.S. Son, J.S. Park, T.S. Kim, R. Choi, J.K. Jeong, J.Y. Kwon, B. Koo and S. Lee, Appl. Phys. Lett. **95** (23), 232106 (2009).
[6] K. Nomura, T. Kamiya and H. Hosono, Adv. Mater. **23** (30), 3431 (2011).
[7] J.K. Jeong, H.W. Yang, J.H. Jeong, Y.G. Mo and H.D. Kim, Appl. Phys. Lett. **93** (12), 123508-1 (2008).
[8] J.P. Lee, J.Y. Hwang and B.S. Bae, J. Semicond. Tech. Sci. **35** (1), 72 (2014).

[9] J.W. Lee, S.Y. Kim, S.O. Kim, H.S. Oh, J.E. Pi, C.S. Hwang and K.C. Park, J. Inf. Disp. **15** (4), 207 (2014).
[10] B. Kim, C.I. Ryoo, S.J. Kim, J.U. Bae, H.Y. Seo, C.D. Kim and M.K. Han, IEEE Electron Dev. Lett. **32** (2), 158 (2011).
[11] A. Suresh, P. Wellenius, V. Baliga, H. Luo, L.M. Lunardi and J.F. Muth, IEEE Electron Dev. Lett. **31** (4), 317 (2010).
[12] J.M. Lee, I.T. Cho, J.H. Lee and H.I. Kwon, Jpn. J. Appl. Phys. **48** (10R), 100202-1 (2009).
[13] T.H. Hwang, I.S. Yang, O.K. Kwon, M.K. Ryu, C.W. Byun, C.S. Hwang and S.H.K. Park, Jpn. J. Appl. Phys. **50** (3s), 03CB061-4 (2011).
[14] H. Luo, P. Wellenius, L. Lunardi and J.F. Muth, IEEE Electron Dev. Lett. **33** (5), 16 (2013).
[15] M.J.M. Pelgrom, A.C. Jeannet, V. Rens, M. Vertregt and M.B. Dijkstra, IEEE J. Solid-State Circ. **29** (8), 879 (1994).
[16] A. Dey and D.R. Allee, *Proceedings Custom Integrated Circuits Conference*, 2012 IEEE, San Jose, CA, USA, 2012, pp. 1–4.
[17] T.C. Huang, Y.H. Yeh and K.T. Cheng, *Symposium Digest of Technical Papers: Flexible Electronics and Displays* (Industrial Technology Research Institute, Hsinchu, 2008), pp. 60–61.
[18] A. Jamshidi-Roudbari, P.C. Kuo and M.K. Hatalis, Solid-State Electron. **54** (4), 410 (2010).
[19] J.P. Bermundo, Y. Ishikawa, H. Yamazaki, T. Nonaka and Y. Uraoka, ECS J. Solid State Sci. Technol. **3** (2), 16 (2013).
[20] S.G. Uppili, D.R. Allee, S.M. Venugopal, L.T. Clark and R. Shringarpure, *Flexible Electronics & Displays Conference and Exhibition*, 2009 IEEE, Phoenix, AZ, USA, 2009, pp. 1–5.