Electrical Characteristics of a-IGZO TFTs With SiO_2 Gate Insulator Prepared by RF Sputtering

Jin-Kuk Kim, So-Hyun Jeong, Sang-A Oh, Seung-Jae Moon, Kimihiko Imura, Tatsuya Okada, Takashi Noguchi, Eui-Jung Yun, and Byung Seong Bae

***Abstract*—This study examined the electrical properties of a-IGZO thin-film transistors (TFTs) with a gate insulator of SiO_2, in which a more TFT-industry-compatible sputtering technique was used for all processing steps. Instead of plasma enhanced chemical vapor deposition, a room-temperature sputtered SiO_2 gate insulator was used, which is more preferable for the simple and low cost process for oxide TFTs. The dielectric strength of the sputtered SiO_2 film with an oxygen ratio of 6.25% was 6.3 MV/cm, which is sufficient for a gate insulator. The a-IGZO TFTs with the sputtered SiO_2 gate insulators showed the optimal device parameters after post-annealing at 400°C for 1 hour in air: saturation field-effect mobility of 3.80 $cm^2/V \cdot s$, V_{th} of −2.84 V, on/off ratio of 1.43×10^5, and $S.S$ of 0.88 V/dec.**

***Index Terms*—Gate insulator, indium-gallium-zinc oxide (IGZO), oxide thin-film transistor (TFT), RF sputtering, SiO_2.**

I. Introduction

TRANSPARENT amorphous indium-gallium-zinc oxide thin-film transistors (a-IGZO TFTs) have attracted considerable attention as a switching device for flat-panel displays. Oxide TFTs are appropriate for organic light-emitting diode (OLED) and flexible electronics because they exhibit a higher field effect mobility than amorphous silicon TFTs, good transparency with a wide band gap and can be processed at low-temperatures [1]–[5]. For TFTs, chemical vapor deposition (CVD) has been adapted widely for depositing semiconductor channel and gate insulator films on large-area glass substrates. On the other hand, CVD is unsuitable for deposition on a plastic substrates because of its high deposition temperature. The TFT process temperature needs to be lower than 200 °C for the development of oxide TFTs on both glass and plastic substrates [6]–[8]. Sputtering is suitable for the fabrication of TFTs on plastic substrates because deposition can be carried out at room temperature. On the other hand, high-temperature post annealing is still necessary for the best performance of IGZO TFTs. Therefore, flexible application, low temperature annealing with high performance is needed. Several studies have been tried to improve properties of silicon oxide films by changing the sputtering conditions, such as reactive gas in argon gas. They improved the properties of silicon oxide films, such as surface texture and dielectric strength [9]–[11]. In addition, poly-Si TFTs using silicon oxide films deposited by sputtering at low-temperature [12]–[14] and a study of the application of various metal oxide TFTs have also been reported [15]–[18]. Despite this, the application of oxide TFTs with sputtered SiO_2 has not been reported. This study investigated the electrical properties of a-IGZO TFTs with a gate SiO_2 insulator deposited by RF sputtering, and the mobility up to 3.80 $cm^2/V \cdot s$ was obtained with optimized sputtering condition of gate insulator such as oxygen ratio to Ar.

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II. Experiment Details

Two kinds of sample were fabricated; a MOS structure to study the electrical characteristics of the insulator and an oxide TFT to study the effects of the insulator.

The MOS structure was fabricated on a p-type silicon wafer. The SiO_2 films were deposited by RF magnetron sputtering with oxygen ratios of 0%, 6.25%, and 18.75% during the deposition. An Al electrode was deposited by thermal evaporation through a shadow mask.

The bottom gate structure of the a-IGZO TFTs with the SiO_2 dielectric film was fabricated on a glass substrate. Fig. 1(a) shows the schematic structure of the fabricated TFT. Mo (150 nm) was deposited on the glass substrate by DC magnetron sputtering and patterned by wet etching as a gate electrode. Subsequently, a dielectric layer of SiO_2 (300 nm), channel layer of a- IGZO (50 nm) and etch-stopper layer (ESL) of SiO_2 (150 nm) were deposited sequentially by RF magnetron sputtering. Here, we emphasize that some samples with the same structure were fabricated without the etch-stoper layer to explore the effects of ESL on the stability properties of the fabricated TFTs. The SiO_2 was deposited at room temperature using a SiO_2 target under the following conditions: RF power of 150 W, working pressure of 2 mtorr and O_2 ratio of 6.25%. The a-IGZO of the channel layer was deposited at 200 °C using a target of In:Ga:Zn = 1:1 : 1 in atomic ratio under the following conditions: RF power of 50 W, working pressure of 5 mtorr and O_2 ratio of 25%. SiO_2 and a-IGZO were post-annealed at 400 °C for 1 hour in air after deposition. An etch-stopper layer and channel region were then patterned by dry and wet etching, respectively. Finally, the Al source-drain electrodes (150 nm) were deposited by DC magnetron sputtering and patterned by

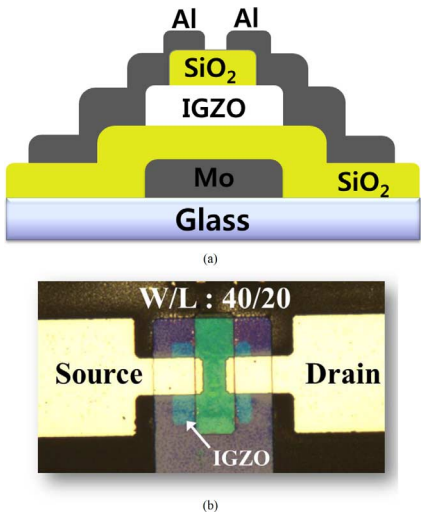

Fig. 1. (a) Schematic cross-sectional view and (b) photographic top view of sputter-deposited a-IGZO TFTs with a sputtered SiO_2 gate insulator developed in this work: $W = 40\ \mu$m and $L = 20\ \mu$m.

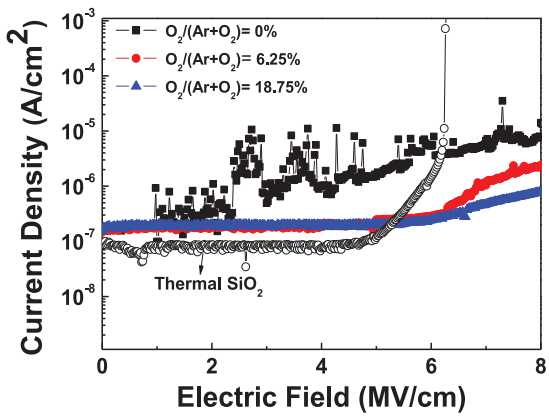

Fig. 2. Current density-electric field (C-E) characteristics as a function of the oxygen content introduced during film deposition, which were obtained from the metal/sputtered-SiO_2/p-type Si MOS capacitors. The same characteristics for the thermally-grown SiO_2 are also shown in the figure for comparison.

wet etching. Fig. 1(b) presents optical microscopy images of the a-IGZO TFT. The channel width (W) and length (L) were 40 μm and 20 μm, respectively.

III. Results and Discussion

Fig. 2 shows the measured current density versus the electric field for the SiO_2 layers with various oxygen contents during sputtering. The currents were measured with the metal/sputtered-SiO_2/p-type Si MOS structures. As shown in Fig. 2, the current density decreased with increasing oxygen ratio, and the dielectric strength of the sputtered SiO_2 films was improved by increasing the oxygen ratios. This result is similar to that reported by Suyama *et al.* [9], who showed that the dielectric strength of SiO_2 films was increased by the existence of larger amounts of oxygen in the sputtering gas. Fig. 2 also shows that the dielectric strenth of 6.3 MV/cm for the sputtered SiO_2 films with an oxygen ratio of 6.25% was comparable to that of the thermally-grown SiO_2 films. This suggests that the sputtered SiO_2 films prepared in this study have a sufficient quality for use as a gate insulator.

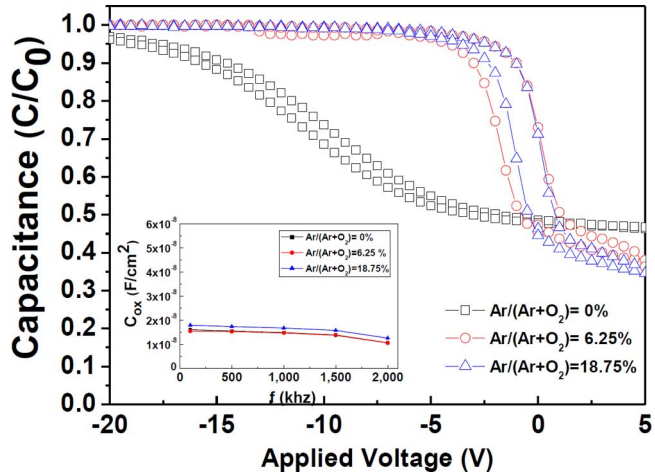

Fig. 3. Hysteresis of the normalized capacitance–voltage (C–V) characteristics as a function of the oxygen contents for the MOS structures measured at 500 kHz. The inset in the figure also shows the C-frequency characteristics as a function of the oxygen content.

To evaluate the quality of the sputtered SiO_2 films further, the hysteresis of normalized capacitance-voltage characteristics as a function of oxygen contents for MOS structures at various frequencies ranging from 100 kHz to 2 MHz and those measured at 500 kHz are shown in Fig. 3. The flat-band voltage became less negative for the SiO_2 films deposited at a higher oxygen ratio. For the films deposited at a higher oxygen ratio, the transition from accumulation to inversion occurred more rapidly, and the hysteresis was reduced further. These results suggest that the positive defect charges within the SiO_2 film and at the Si/SiO_2 interface decrease for the SiO_2 films prepared with higher oxygen ratios because the positive defect charges in the insulator and at the semiconductor-oxide interface induce an equivalent negative charge in the semiconductor. Therefore, for more defect charges existing within the SiO_2 film and at the Si/SiO_2 interface, a more negative voltage needs to be applied to the metal to obtain the flat band condition and a slower transition between a high capacitance and a low capacitance is observed [19]. The values of high capacitance at 500 kHz in accumulation condition were 15.5, 15.3, and 17.4 nF/cm^2 for samples with oxygen ratios of 0, 6.25, and 18.75%, respectively. The dielectric constant of the sputtered SiO_2 films with an oxygen ratio of 6.25%, which was deduced from the high capacitance values, was 3.46, which is comparable to that of the thermally-grown SiO_2 film.

Fig. 4 presents the transfer characteristics of the amorphous In–Ga–ZnO (a-IGZO) TFTs with a thermal oxide gate insulator (GI) and a SiO_2 GI sputtered with an O_2 mixing ratio of 6.25%. As shown in Fig. 4, similar transfer characteristics were observed with the exception of the off-current. The off-current of TFT with a sputtered SiO_2 GI was higher than that of the TFTs with a thermal SiO_2 GI, suggesting that a thermally deposited SiO_2 film is likely to be denser than a sputtered oxide.

Fig. 5(a) and 5(b) shows the output characteristics as a function of the gate-to-source voltage (V_{GS}) along with the transfer characteristics as a function of the drain-to-source voltage (V_{DS}) for a-IGZO TFTs with a SiO_2 GI sputtered with an O_2 mixing ratio of 6.25%, a 150-nm-thick SiO_2 etch stopper layer

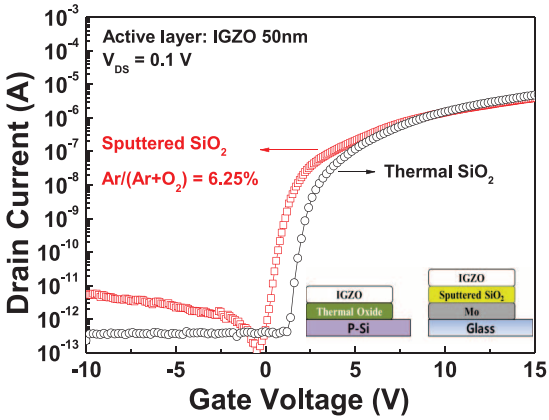

Fig. 4. Comparison of the transfer characteristic of a-IGZO TFTs with a SiO_2 gate insulator sputtered by O_2 of 6.25% on that of TFTs with a thermally-grown SiO_2 gate insulator.

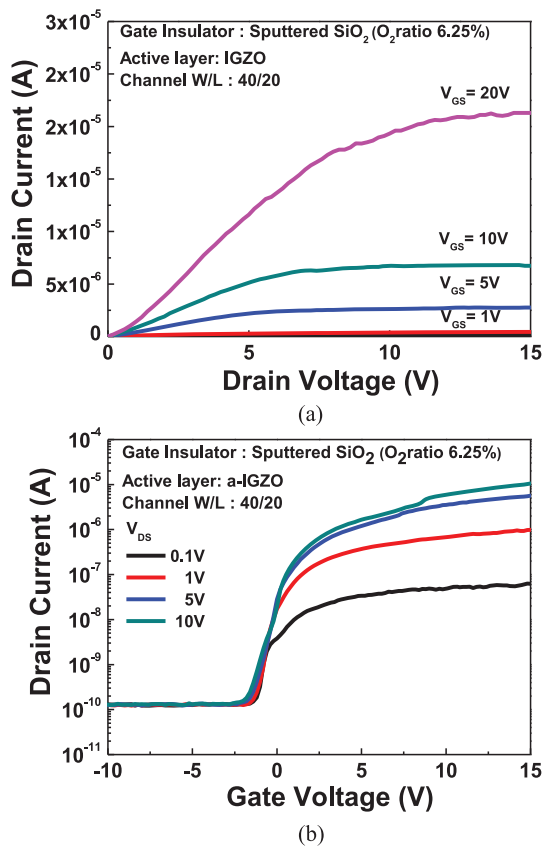

Fig. 5. (a) Output characteristics as a function of the V_{GS} and (b) transfer characteristics as a function of V_{DS} for a-IGZO TFTs with a sputtered SiO_2 gate insulator by O_2 of 6.25%, a 150-nm-thick SiO_2 etch stopper layer, and a W/L ratio of 40/20.

and a channel width (W)/channel length (L) ratio of 40/20. All measurements were taken after post-annealing at 400 °C for 1 hour in air. Fig. 5(a) presents the current-crowding characteristics, suggesting the existence of huge contact resistance between the source/drain electrode and the IGZO channel. Therefore, this contact resistance should be improved to realize TFTs with the best performance. As shown in Fig. 5(b), the measurements were made for various drain voltages and could be classified as the linear region for low drain voltages and

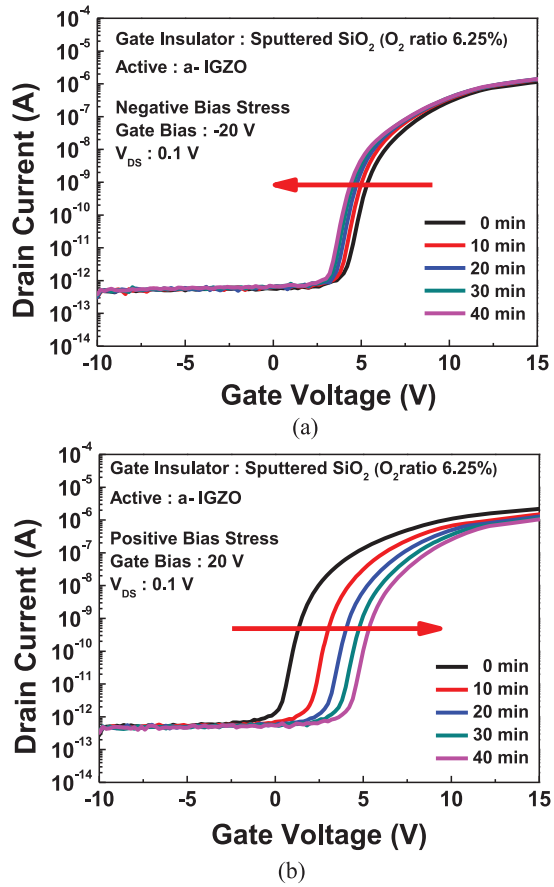

Fig. 6. Transfer characteristics under (a) negative bias stress (NBS) with V_{GS} of -20 V and (b) positive bias stress (PBS) with V_{GS} of 20 V of a-IGZO TFTs with a sputtered SiO_2 gate insulator by O_2 of 6.25% and without an etch stopper layer.

the saturation region for large drain voltages. The slope of the sub-threshold swing $(S.S)$, which describes the change in V_{GS} that should be applied to devices to increase I_{DS} by an order of magnitude, was obtained from the inverse slope of the curve in Fig. 5(b). The linear and saturation field-effect mobilities were also estimated using (1) and (2), respectively

$$\mu_{\text{lin}} = \frac{\partial I_{\text{DS}}}{\partial V_{\text{GS}}} \times \frac{L}{C_{0x} W V_{\text{DS}}} \tag{1}$$

$$\mu_{\text{sat}} = \left(\frac{\partial \sqrt{I_{\text{DS}}}}{\partial V_{\text{GS}}} \right)^2 \times \frac{2L}{C_{\text{ox}} W} \tag{2}$$

where C_{ox} is the capacitance per area of the sputtered SiO_2 GI, which was 15.3 nF/cm^2 measured with a metal-insulator-highly doped semiconductor configuration, as mentioned above. Table I lists the important device parameters of the sputter-deposited IGZO based TFTs, which were obtained from the results shown in Fig. 5(b) using (1) and (2). As listed in Table I, the a-IGZO TFTs with a sputtered SiO_2 GI fabricated on glass substrates and post-annealed at 400°C for 1 hour in air showed the best device parameters, which include a saturation field-effect mobility of 3.80 cm^2/V·s, threshold voltage (V_{th}) of -2.84 V, on/off ratio of 1.43×10^5, and $S.S$ of 0.88 V/dec.

To evaluate the V_{GS}–dependent instabilities of a-IGZO TFTs with a SiO_2 GI sputtered with an O_2 mixing ratio of 6.25% and

TABLE I
SUMMARY OF THE IMPORTANT DEVICE PARAMETERS OF SPUTTER-DEPOSITED IGZO-BASED TFTS OBTAINED FROM THE RESULTS IN FIG. 5(B) USING (1) AND (2)

V_{ds}[V]	V_{th} [V]	S.S [V/dec]	I_{on}/I_{off}	μ_{lin} [cm^2/v·s]
0.1	-1.33	0.58	4.72×10^2	2.06
1	-1.57	0.68	9.17×10^3	2.35
5	-1.77	0.87	6.15×10^4	2.94
V_{ds}[V]	V_{th} [V]	S.S [V/dec]	I_{on}/I_{off}	μ_{sat}[cm^2/v·s]
10	-2.02	0.90	1.11×10^5	3.11
20	-2.84	0.88	1.43×10^5	3.80

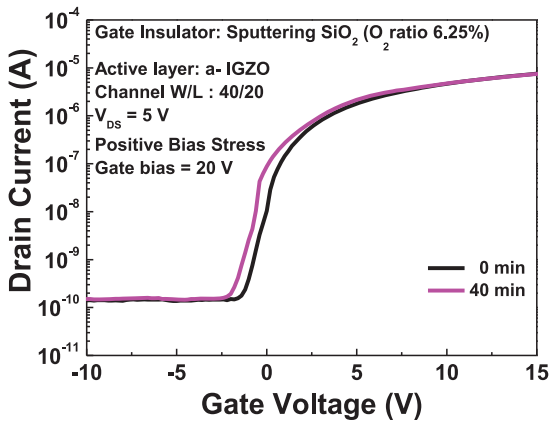

Fig. 7. Transfer characteristics of a-IGZO TFTs with a SiO_2 etch stopper layer under a positive bias stress (PBS) with V_{GS} of 20 V.

without an etch stopper layer, their transfer characteristics under negative bias stress (NBS) with $V_{GS} = -20$ V and positive bias stress (PBS) with $V_{GS} = 20$ V were measured, as shown in Fig. 6(a) and 6(b), respectively. As shown in Fig. 6(a), with increasing NBS stress time, the shape of the transfer characteristics was unchanged, even though the V_{th} had shifted slightly to the negative direction. On the other hand, Fig. 6(b) shows the V_{th} shift by 4.15 V after a PBS stress time of 40 min, whereas the other parameters are likely to be unchanged. This suggests that the PBS-induced instability was more severe than the NBS one for a-IGZO TFTs without an etch stopper layer. The V_{GS}-induced instability of the IGZO TFTs has been attributed to charge trapping at the interface between a GI and a channel layer, the interfacial trap charges, and/or the absorption/desorption of ambient elements, such as oxygen and water molecules, on the surface of a-IGZO channel [20], [21].

This ambient effect can be excluded using an etch stopper layer deposited on the channel layer, which acts as a passivation layer. Fig. 7 presents the transfer characteristics of the a-IGZO TFTs with a 150-nm-thick SiO_2 etch stopper layer under PBS with $V_{GS} = 20$ V, which suggests that the PBS-induced instability of the IGZO TFTs was suppressed by the deposition of an etch stopper layer. Therefore, based on the results shown in Figs. 6(b) and 7, the V_{GS}–induced instability of the IGZO TFTs prepared in this study was due mainly to the absorption/desorption of ambient elements, such as oxygen and water molecules, on the surface of the a-IGZO channel.

IV. CONCLUSION

The electrical characteristics of a-IGZO TFTs with a gate insulator of SiO_2 deposited by a more TFT-industry-compatible sputtering process were demonstrated. The dielectric strength of 6.3 MV/cm observed for the sputtered SiO_2 gate insulators with an oxygen ratio of 6.25% was comparable to that of the thermally-grown SiO_2 films, which suggests that the prepared SiO_2 gate insulators have sufficient quality as a gate insulator. From the capacitance-voltage properties of the sputtered SiO_2 gate insulators, it was concluded that the gate insulators prepared with higher oxygen contents contained smaller amounts of positive defect charges. The a-IGZO TFTs with a sputtered SiO_2 gate insulators fabricated on glass substrates and post-annealed at 400 °C for 1 hour in air exhibited the best device parameters, which include a saturation field-effect mobility of 3.80 $cm^2/V \cdot s$, threshold voltage of -2.84 V, on/off ratio of 1.43×10^5, and $S.S$ of 0.88 V/dec. The PBS-induced instability was more severe than the NBS one for the a-IGZO TFTs without an etch stopper layer. Overall, the V_{GS}–induced instability of the IGZO TFTs prepared in this study was due mainly to the ambient effects.

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