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Development of ZnO-based Thin-film Transistors with Top Gate Structures

Eui-Jung Yun*
Department of Semiconductor and Display Engineering and Department of System Control Engineering, Hoseo University, Asan 336-795, Korea

Hye Ji Moon
Department of Semiconductor and Display Engineering, Hoseo University, Asan 336-795, Korea

Byung Seong Bae
Department of Semiconductor and Display Engineering and College of New IT Engineering, Hoseo University, Asan 336-795, Korea

Sun-Moon Jin, Hyoung G. Nam and Nam-Ihn Cho
Electronic Engineering Division, Sun Moon University, Asan 336-708, Korea

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Zinc oxide (ZnO)-based thin-film transistors (TFTs) with top gate structures were produced. Radio-frequency-magnetron sputtering was used to deposit indium tin oxide for both the source and the drain electrodes and n-type undoped ZnO at high oxygen partial pressures for the active layer. Direct-current-magnetron sputtering and plasma enhanced chemical vapor deposition were used to deposit Al for the gate electrode and the SiN gate dielectric, respectively. The devices operated in the enhancement mode with a threshold voltage, mobility, on-off ratio and sub-threshold slope of 9 V, 0.05 cm^2/Vs, $\sim 5 \times 10^5$, and 1.3 V/decade, respectively.

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I. INTRODUCTION

Thin-film transistors (TFTs) have provided the opportunity to develop display technologies, wearable electronics and large-area memories [1–3]. Zinc oxide (ZnO) thin films have also been considered a promising engineering material for the fabrication of TFTs on glass or polymer substrates because ZnO active layers in TFTs offer high channel mobility, high optical transparency and insensitivity to visible light, and higher driving currents. In addition, they can be fabricated by sputtering at room temperature [4–6].

Despite the continued improvement in the TFT performance, many factors are not completely understood, one of them being the selection of the device structure. As a device structure, many candidates, such as the bottom gate with a top contact [2-4,6-12] and the bottom gate with a bottom contact [5,13], have already been studied. On the other hand, there are few reports on the development of ZnO-based TFTs employing a top gate as the device structure [1,14]. Li *et al.* [1] reported that top-gate-type TFTs with undoped ZnO as the active channel layer can show N-channel depletion-mode operation. Recently, Jun *et al.* [14] reported that top-gate flexible TFTs with active layers formed by the spin-coating of ZnO nanoparticles operated in the enhancement mode with a very low field-effect mobility and a low on-off ratio of 1.2×10^{-5} cm^2/Vs and 1.5×10^3, respectively. This study developed another ZnO-based TFT with a top gate structure by using the following procedures: radio-frequency-magnetron sputtering (RFMS) to deposit indium tin oxide (ITO) for the source and drain electrodes and undoped ZnO for the active layer, plasma enhanced chemical vapor deposition (PECVD) to prepare SiN for the gate dielectric, and direct-current-magnetron sputtering (DCMS) to deposit Al for the gate electrode.

II. EXPERIMENTAL

ZnO-based TFTs were developed using a top gate structure with an Al gate electrode and an undoped ZnO

*E-mail: ejyun@hoseo.edu; Tel: +82-41-5405675; Fax: +82-41-5405587

Table 1. Summary of the deposition conditions for all layers in the ZnO-based TFT devices prepared in this study.

Parameter	Deposition Condition			
	Source/Drain Electrodes ITO	Gate Electrode Al	Gate Dielectric SiN	Active Layer ZnO
Deposition Method	RF Magnetron Sputtering	DC Magnetron Sputtering	PECVD	RF Magnetron Sputtering
Target	ITO	Al	–	ZnO
Reaction Gas	Ar (99.999%)	Ar (99.999%)	20% SiH_4/He (100 sccm), N_2 (2000 sccm), NH_3 (160 sccm)	Ar (99.999%) O_2 (99.999%)
O_2 Fraction [O_2/(O_2 + Ar)]	0 (Ar only)	0	–	0.67
Total Gas Pressure (mTorr)	2	5	2000	20
Substrate Rotation (rpm)	0	0	0	5
Substrate Temperature (°C)	200	RT	350	500
Power (W)	50	125	1.5	240
Film Thickness (nm)	100	150	250	50

active layer. Five materials were used in this process, silica, Al, SiN, ZnO and ITO for the substrate, gate electrode, gate dielectric, active layer, and source and drain electrodes, respectively.

The TFTs were implemented on corning glass substrates that had been solvent cleaned prior to being loading into the RFMS system. To produce the source and drain contact electrodes, we deposited a conducting ITO film onto 498-μm-thick corning glass substrates by using the RFMS from an ITO target. Ar (99.999% pure) was used as the reaction gas to generate the Ar plasma. The total gas pressure was 2 mTorr. The substrate was in the static mode and was heated to 200 °C during deposition. The ITO target power was 50 W. Typical ITO film thicknesses were approximately 100 nm. After the photoresist pattern had been processed, the patterns for the source and the drain contact electrodes were defined by wet etching using dilute nitric acid (1%). Subsequently, a semi-conducting undoped ZnO film, which is the active layer with a thickness of approximately 50 nm, was deposited onto the ITO source and drain contacts by using the RFMS from a 99.99%-pure ZnO target by using mixtures of 99.999% pure Ar and O_2 gases as the reaction gases. The O_2/(O_2 + Ar) fraction and the total gas pressure were 0.67 and 20 mTorr, respectively. The substrate was also rotated at 5 rpm and heated to 500 °C during the deposition. The ZnO target power was fixed to 240 W. The gate dielectric, SiN, was deposited to a thickness of 250 nm in a PECVD system at 350 °C. SiH_4/Ne (20%, 800 sccm), N_2 (2000 sccm), and NH_3 (160 sccm) were used as the reaction gases. The total gas pressure was 2000 mTorr. The system power was fixed to 1.5 W. Subsequently, the gate dielectric patterns were formed by reactive ion etching. Finally, a gate-contact electrode, Al, was sputter deposited by using the DCMS process at room temperature (RT) and was defined by wet etching using an Al etchant. Table 1 lists the deposition conditions for all layers in the TFT devices fabricated in this study.

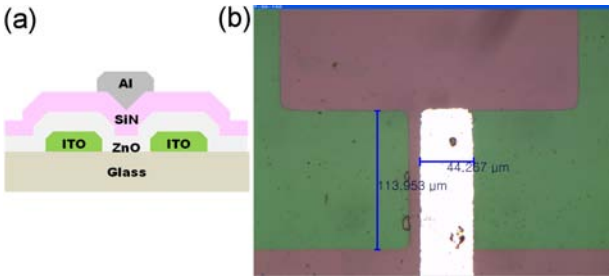

Fig. 1. (Color online) (a) Schematic cross-sectional view and (b) plane view of the ZnO-based TFTs developed in this study: W = 100 μm and L = 50 μm.

Figures 1(a) and 1(b) show a schematic cross-sectional view and plane view of the typical ZnO-based TFTs developed in this study, respectively. As shown in Fig. 1, the TFTs had a top gate structure. The channel width (W) and the channel length (L) were varied from 100 to 200 μm and from 10 to 50 μm, respectively. The gate dielectric in a TFT should be planar and free of surface roughness and defects at the gate dielectric/active layer interface, which leads to a decrease in the gate leakage and in the interface scattering [3].

The device characteristics of the ZnO-based TFTs were measured at RT in the dark in air by using two Keithley 2400 source meters for the DC voltage source and a Keithley 6485 picoammeter for the current measurement along with the corresponding software (Microsoft visual basic). The capacitances of the SiN gate dielectric films were measured at RT by using an Agilent 42854A precision LCR meter after forming Ohmic contacts with a 150-nm-thick molybdenum (Mo) layer by using DCMS.

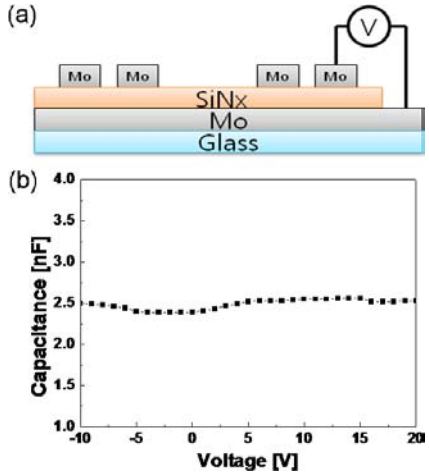

Fig. 2. (Color online) (a) Schematic cross-sectional view and (b) capacitance-voltage (C-V) characteristics of the SiN (250 nm) capacitor with Mo as the two electrodes used to evaluate the capacitance per area (C_{SiN}) of the SiN gate dielectric material.

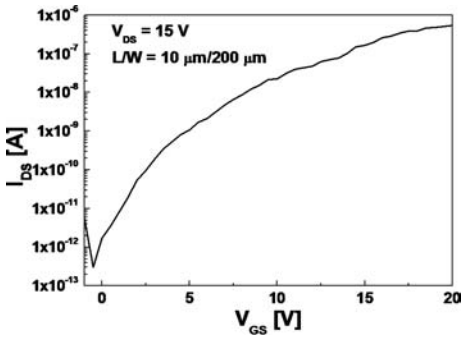

Fig. 3. Typical I_{DS}-V_{GS} transfer characteristics of the ZnO-based TFTs with W/L dimensions of 200 μm/10 μm at a fixed V_{DS} of 15 V.

III. RESULTS AND DISCUSSION

Figure 2(a) shows a schematic cross-sectional view of the SiN (250 nm) capacitor with Mo used as the two electrodes to evaluate the capacitance per area (C_{SiN}) of the SiN gate dielectric material. Figure 2(b) shows the capacitance-voltage (C-V) characteristics of the SiN capacitor structure. The figure indicates that the PECVD SiN thin films have a C_{SiN} of 1.1×10^{-8} F/cm^2.

Figure 3 shows the typical drain-to-source current *vs.* gate-to-source voltage (I_{DS}-V_{GS}) transfer characteristics of the ZnO-based TFTs with W/L dimensions of 200 μm/10 μm. The I_{DS} was measured in a light-tight box as the V_{GS} was swept from -2 to 20 volts (V). A series of measurements were performed in which the drain-to-source voltage (V_{DS}) was fixed to 15 V, which is in the saturation region. The I_{DS}-V_{GS} characteristics revealed that a positive V_{GS} was needed to enhance the electron carriers in the n-type active layer, which turns on the TFTs. This suggests that these TFT devices operate in the enhancement mode, exhibiting a normally off channel state. Figure 3 also shows that the drain-to-source current in the off state ($I_{DS\ off}$) is approximately 1×10^{-12} A and that the on/off ratio is approximately 5×10^5. The resistivity of the active ZnO layer, ρ, was estimated using the following equation [5]:

$$\rho = \frac{W t_c}{I_{DSoff} L} V_{DS} \quad (\text{at off} - \text{state}), \tag{1}$$

where t_c is the thickness of the active ZnO layer. The estimated ρ obtained from Eq. (1) was 15×10^8 Ωcm. Equation (1) shows that to reduce the leakage current, the W/L ratio and the t_c need to be decreased and that ρ needs to be increased. Enhancement-mode TFTs are preferable for efficient TFT operation over depletion-mode TFTs because the enhancement-mode TFTs do not require a voltage to turn off the TFTs, which leads to much less power dissipation. Li *et al.* [1] reported that ZnO-based TFTs with a top gate structure, in which the undoped ZnO active layer has a low ρ of 10 Ωcm and high a carrier concentration of 10^{18} cm^{-3}, showed N-channel depletion-mode operation. This suggests that the ZnO active layer in the top gate type TFTs should have both a high ρ and a low carrier concentration for enhancement-mode TFT operation. The TFTs in the present study showed enhancement-mode operation due to the very high ρ of 15×10^8 Ωcm and the low carrier concentration.

The sub-threshold characteristics of the ZnO-based TFTs with W/L dimensions of 200 μm/10 μm, which indicate the device performance at V_{GS} lower than the threshold voltage (V_{th}), were also obtained from the inverse slope of the curve in Fig. 3. The slope of the sub-threshold swing (S_{st}), which describes the change in V_{GS} that should be applied to devices to increase I_{DS} by an order of magnitude, can be expressed as follows [3]:

$$S_{st} = \left[\frac{d(\log I_{DS})}{dV_{GS}} \right]^{-1}. \tag{2}$$

A typical S_{st} for the developed TFTs obtained from the result in Fig. 3 was approximately 1.3 V/decade.

The maximum I_{DS} at the saturation region ($I_{DS,sat}$) is generally independent of V_{DS} and can be expressed by using the following equation:

$$I_{DS,sat} = \frac{W \mu_{FE} C_{SiN}}{2L} (V_{GS} - V_{th})^2 \quad (\text{for } V_{DS} > V_{GS} - V_{th}), \tag{3}$$

where μ_{FE} is the field effect electron mobility inside the n-type channel formed in the n-type ZnO active layer, and C_{SiN} is the capacitance per area of the SiN gate dielectric material. Figure 2 shows that C_{SiN} was 1.1×10^{-8} F/cm^2.

Figure 4 presents the $I_{DS}{}^{1/2}$ *vs.* V_{GS} curve of the developed TFTs obtained from the result in Fig. 3 by using Eq. (3). To estimate μ_{FE}, we substituted the slope value

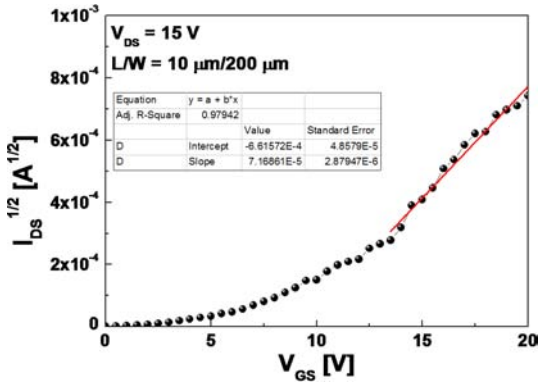

Fig. 4. (Color online) ${I_{DS}}^{1/2}$ versus V_{GS} curve of the developed TFTs obtained from the result in Fig. 3 by using Eq. (3).

of the linear portion of the curve in Fig. 4 into Eq. (3). In Fig. 4, an extrapolation method [3,5] was also used to determine V_{th}. Based on the average characteristics of more than 10 devices, μ_{FE} and V_{th} were found to be 0.05 cm^2/Vs and 9 V, respectively. The μ_{FE} values estimated in this study were lower than the field effect electron mobility (31 cm^2/Vs) [9] obtained from the TFTs with a bottom gate structure by using PECVD-grown SiN and rf-sputtered undoped ZnO as the gate dielectric and the active layer, respectively. The reason for this is that the ZnO active layer in the top gate structure was exposed to the SiN-PECVD process because it was performed before the gate dielectric deposition step, which can lead to an increase in ρ in the active layer, resulting in a decrease in μ_{FE} based on the equation, $\mu_{FE} = 1/(nq\rho)$, where q is the charge of an electron and n is the carrier concentration. On the other hand, Jeong *et al.* [15] reported that TFTs with a bottom gate structure had a V_{th} instability problem due to the interaction between the exposed active layer surface and oxygen and/or water vapor in the ambient atmosphere, suggesting that a suitable passivation layer is essential to improve the long-term reliability of the ZnO-based TFTs with a bottom gate structure. Therefore, both the top gate structure and the optimized ZnO active layer (reasonably high resistivity and low carrier concentration) are essential for developing high-performance ZnO-based TFTs.

IV. CONCLUSION

New ZnO-based TFTs with a top gate structure that employs SiN and undoped ZnO as a gate dielectric and an active layer, respectively, were developed. The I_{DS}-V_{GS} transfer characteristics of the new ZnO-based TFTs showed that the TFT devices operated in the enhancement mode and exhibited a low $I_{DS\ off}$ of approximately 1×10^{-12} A and a good on/off ratio of 5×10^5. These TFTs showed enhancement-mode operation due to the very high ρ value of 15×10^8 Ωcm and the low carrier concentration. The sub-threshold characteristics of the developed ZnO-based TFTs also exhibited a good S_{st} of approximately 1.3 V/decade. The ${I_{DS}}^{1/2}$ *vs.* V_{GS} curve of the developed TFTs showed that μ_{FE} and V_{th} were 0.05 cm^2/Vs and 9 V, respectively. The low μ_{FE} values estimated in this study were attributed to an increase in ρ in the ZnO active layer, which had been exposed to the SiN-PECVD process. Overall, both the top gate structure and the optimized ZnO active layer are important for developing ZnO-based TFTs with high performance.

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